Synthesis of a New Class of Converters That Utilize Energy Recirculation

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Abstract — A new class of switchmode power electronic circuit topologies, here in named Energy Recirculation and Storage Circuits (ERSCs), are described which have the characteristic of storing and recirculating energy in a return path to augment the source. A port reduction technique is developed which connects output to input and is applied to buck and boost derived converters. A description of circuit operation is given for an ideal boost/buck ERSC.

Two possible applications for ERSCs are for in-situ testing of power devices and for power factor correction. The second utilizes a cascaded boost/buck ERSC as an output-regulated power-factor correction (PFC) circuit. The PFC-ERSC is evaluated and a detailed description with key equations included.

Introduction

The late Peter Wood described in a 1989 EPRI report [1] the concept of a converter which returned output energy to the input to augment source capacity. This created a greater power flow within the converter and allowed testing of semiconductor devices at power levels higher than available from the source. This same concept was utilized recently by Heumann, Kellar and Sommer [2] in a "novel circuit" for testing IGBT devices. A more general application of the *concept* has been described by Singer [3], who presents an active "loss-free resistor" which is used to return energy to an alternate position in the circuit or to the source. And Kheraluwala, Steigerwald and Gurumoorthy [4] *present a transient* boost supply which uses a transformer-coupled resonant boost stage to inject circuit current in series with the source.

The concept of "recirculating energy" has much broader application and can be used to devise a new family of converters that have application to power-factor correction, capacitor charging, bi-directional power flow, increasing transient response, etc. The concept is fundamental, in that it describes a method to achieve a second degree of freedom in control by providing a second path for power flow.

In this paper the concept is applied to buck and boost derived topologies to show an evolution of a family of circuits, herein named *Energy Recirculation and Storage Circuits* (ERSCs). This paper, which summarizes recent research [5], presents the development of connection rules to form an ERSC; evolution of a complete family of single- and double-ended circuits; state equations for the family of converters; description and verification of operation of an ideal boost/buck derived ERSC; and application to power factor correction. The extension of this to resonant topologies [5,6] is not included.

Synthesis of ERSCs

All ERSC topologies are synthesized from two-port, ladder-structured buck and boost derived dc/dc switchmode power converter topologies. These topologies are derived from the reduction of two-port power converters to single port topologies. The derivation consists of matching port characteristics and appropriately connecting the output port to the input, exclusive of a load, to create a recirculation and storage of energy. The recirculated energy is added to the input energy and is used to simulate a higher power source.

These ladder structured converters are comprised of two or more sections depending upon the complexity of the converter. The more complex converters have an input section, one or more middle or energy buffer sections, and an output section [7]. The input and output port characteristics are of great importance when applying the port reduction technique. The *input section contains* an input power source and an active switch. The source can either be a real or effective constant-voltage or constant-current source. For example, an effective voltage source is a real current source placed in parallel with a large filter capacitor while an effective current source is generated by the series combination of a real voltage source and a large inductor. In practice, almost all input sources are either real voltage sources or effective current sources. In this paper, all four types of input sources are utilized in the input sections so that exact duality between ERSCs can be established. Real power sources are power limited, i.e. real voltage sources are current limited and real current sources are voltage limited. It is this limited power output that ERSCs are designed to overcome.

Input and output port characteristics are either constant voltage or constant current. Constant-current output, while common in many converters, is often disguised as constant voltage by the placement of a filter capacitor in parallel with the load. Capacitors used as filter elements on the constant current output are omitted, again, to establish exact duality between ERSCs.

There are six basic dc/dc switchmode converter topologies [7]. All six of these converters along with their characteristic circuits are shown in Fig. 1. Circuit duality between the buck and boost converters, the single-

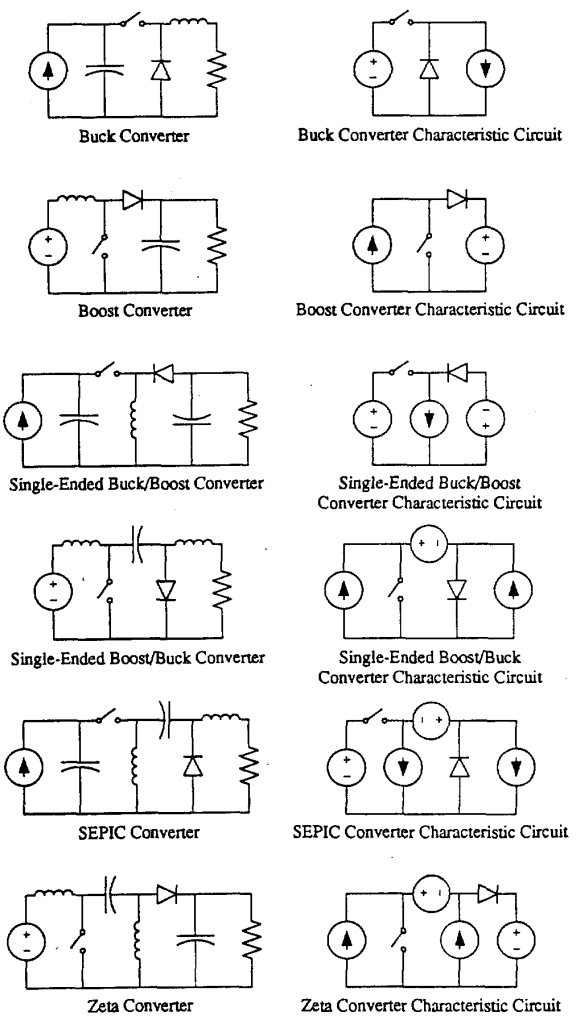

Fig. 1 Basic dc/dc Converters and Characteristic Circuits

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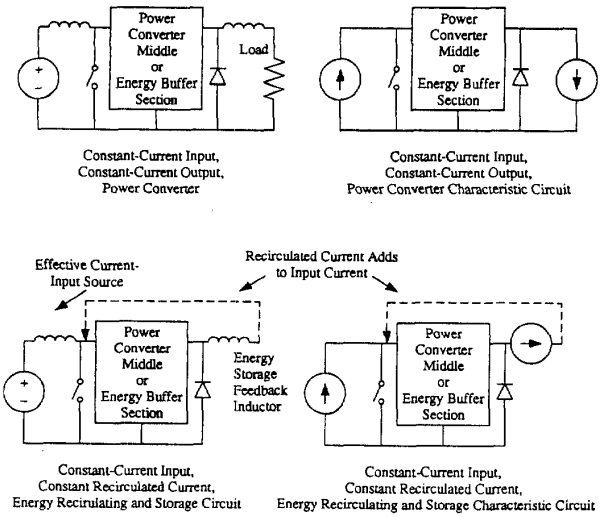


Fig. 2. Constant-Current Port-Reduction Technique
1. Remove load
2. Connect constant-current output to sum with constant-current input at the positive input terminal.

ended buck/boost and single-ended boost/buck converters, and the SEPIC and zeta converters is evident in the pairs of respective characteristic circuits.

Output to Input Connection Rules

The derivation of an ERSC is accomplished through connection of the output to the input in the absence of a load. This connection allows the converter to operate as if it were normally loaded while recirculating and storing all or part of the energy usually delivered to the load. The recirculated energy adds to the input energy increasing the amount of energy processed by the converter. This operation has two topological

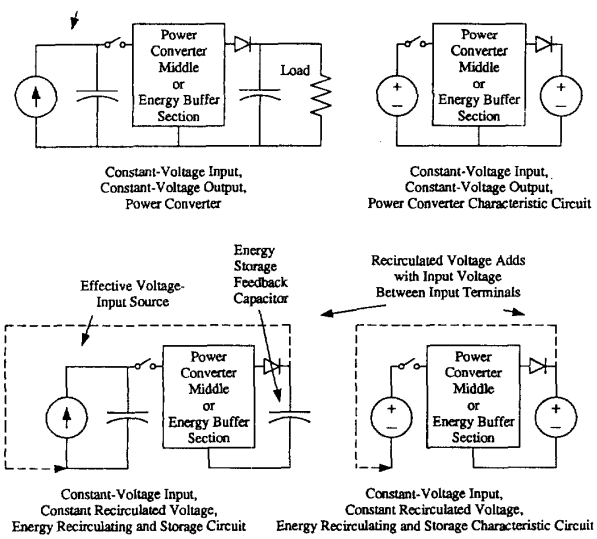


Fig. 3. Constant-Voltage Port-Reduction Technique
1. Remove load.
2. Disconnect voltage input source from negative input terminal.
3. Connect positive output terminal to negative side of input source (vice versa).

requirements. The first is that the output- and input-port characteristics be matched, i.e. if the input characteristic is constant voltage then the output characteristic must be constant voltage. The second is that the ports to be reduced must have a common connection between the input and output. The common connection on non-transformer isolated, ladder-structured converters cannot connect opposite polarity terminals of one port to that of the other.

If the two topological requirements above are met, then one of two types of output to input port connections can be made. If the electrical characteristic of the matched ports is constant current, the port-reduction technique in Fig. 2, is used. The technique follows Kirchoff's laws where the output current is summed with the input current at the positive input terminal. This connection causes the energy transferred to the load to be stored in the feedback inductor of the ERSC. If a constant power is delivered from the source and the energy stored in the buffer section remains unchanged, the energy stored in the inductor increases with time. This increase, indicative of the current flow in the feedback inductor, increases the amount of total power processed by the power circuit and makes the input source appear to have a greater power capability.

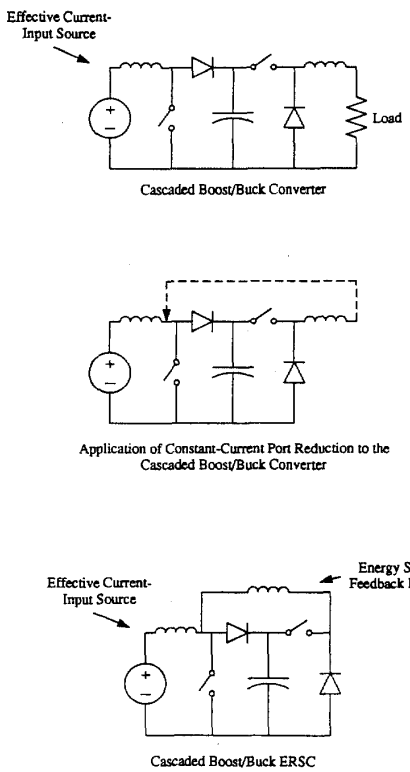


Fig. 4. Synthesis of Cascaded Boost/Buck ERSC

If the electrical characteristic of the matched ports is constant voltage, the port-reduction technique in Fig. 3 is used. The technique follows Kirchoff's laws where the output voltage is connected in series with the input voltage by disconnecting the input source, real or effective, from the negative input terminal and connecting the positive output terminal to the negative side of the input. The energy normally transferred to the load is stored in the feedback capacitor. If the source power and buffer energy are constant, the energy stored in the feedback capacitor increases. This increase in capacitor voltage increases the amount of power processed by the circuit and makes the input source appear to have a greater power capability.

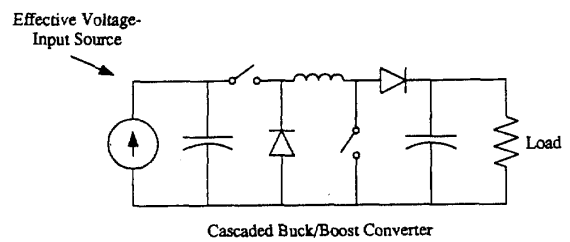
Derived Family of ERSC

The port reduction techniques previously presented are used to synthesize a family of ERSCs from the converters depicted in Fig. 1. The two most basic converters, buck and boost, cannot be port reduced because of the topological requirement for matched ports. Thus, these must be cascaded with another converter to achieve matched port characteristics. The boost converter is cascaded with a buck forming a *Cascaded Boost/Buck ERSC* and can be port reduced using the constant-current port-reduction technique of Fig. 2. The synthesis of the Cascaded Boost/Buck ERSC is presented in Fig. 4.

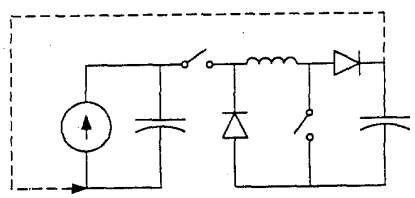
The buck converter is cascaded with a boost to generate a voltage-current-voltage structure and is reduced with the constant-voltage technique of Fig. 3 resulting in the *Cascaded Buck/Boost ERSC* depicted in Fig. 5. The Cascaded Buck/Boost ERSC could have been derived by the dual of the Cascaded Boost/Buck ERSC.

The basic single-ended buck/boost and boost/buck converters in Fig. 1 exhibit a polarity inversion of the output with respect to the input. The common connection between the negative input and positive output terminals make it impossible to form an ERSC directly. A port reduction can be accomplished if transformer-isolated single-ended buck/boost and boost/buck converter topologies [8] are used since input and output terminals of equal polarity can be connected together. The two resulting single-ended ERSCs are shown in Fig. 6. The two-switch cascaded ERSCs can be topologically reduced to single-ended topologies if transformers are used in the energy buffer section and the two active switches are constrained to switch in phase.

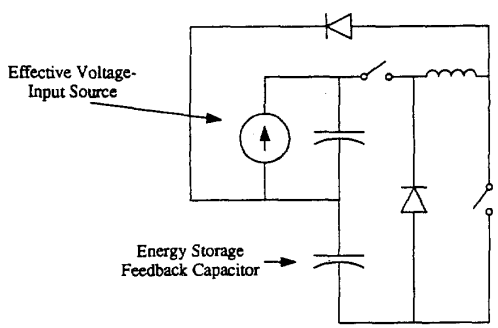
The single-ended ERSCs only have two active switch states while the two-switch topologies have four. The single-ended ERSCs only operate in modes which control the limited electrical characteristic associated with real sources and is the reason that the single-ended topologies are presented with real input sources



Cascaded Buck/Boost Converter



Application of Constant-Voltage Port-Reduction to the Cascaded Buck/Boost Converter



Cascaded Buck/Boost ERSC

Fig. 5. Synthesis of Cascaded Buck/Boost ERSC

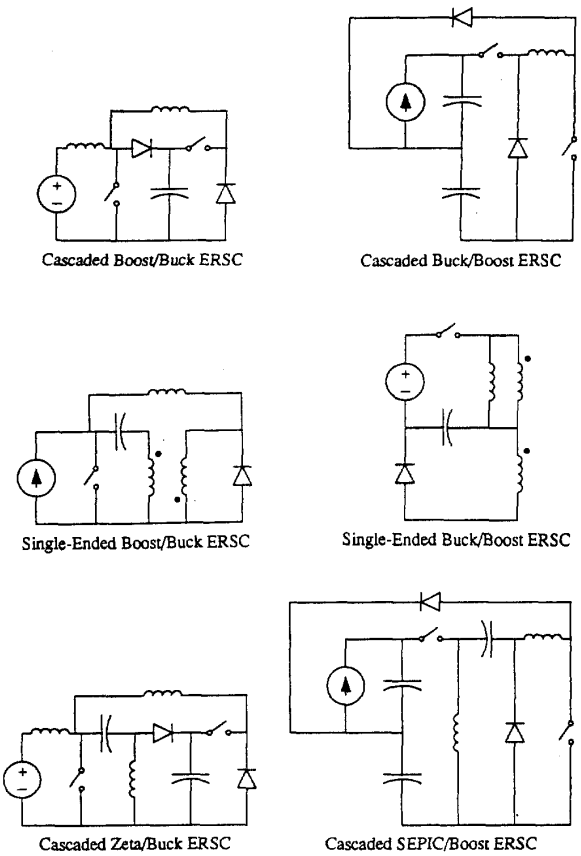


Fig. 6. Buck and Boost Derived Family of ERSCs

The SEPIC and Zeta converters (a single-ended cascade of buck-boost-buck and boost-buck-boost, respectively) are depicted in Fig. 1 and also have unmatched port characteristics. These must be cascaded with another converter to match port characteristics. The SEPIC is cascaded with a boost converter to form a SEPIC/boost cascade which has constant-voltage port characteristics. The Zeta is cascaded with the buck and is port reduced using the constant-current port-reduction technique. The SEPIC converter could be cascaded with a Zeta and vice versa to obtain matched ports.

The entire family of Energy Recirculation and Storage Circuits synthesized from the buck and boost derived converters of Fig. 1 are presented in Fig. 6. Dual ERSC topologies are placed side by side in the figure. The ERSCs which have boost derived inputs and buck derived outputs are on the left. These ERSCs build energy in the feedback inductor and can be used as magnetic storage circuits, transient-boost circuits and for high-current-semiconductor in-situ testing. The ERSCs which have buck derived inputs and boost derived outputs are on the right and charge pump the feedback capacitor. These can be used as charge storage circuits for high-voltage in-situ testing and flash lamp circuits.

Analysis of the Cascaded Boost/Buck ERSC

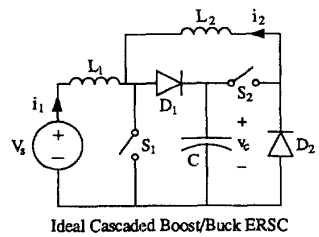
A detailed analysis and description of the top four topologies of Fig. 6 is given in [5]. A detailed description of the operation and analysis of the Cascaded Boost/Buck ERSC and its application to power factor correction is given below.

Because of the energy-pumping characteristic of the ERSC, all operating modes appear transient. Hence, duty cycle is not constant and the use of state-space averaging [9, 10, 11] to analyze the ERSC topologies can not be directly applied. Therefore, the initial development of the ERSCs is approached through analysis of incremental linear transitions of the state variables.

Numerical analysis is used to simulate circuit operation with several assumptions. Currents and voltages in the state equations describing each switch state topology deviate only slightly during switching cycles and the switching frequencies are always much higher than the natural frequencies in each circuit. This causes the state variable transitions to appear linear. Another assumption is that all ERSCs operate in continuous conduction mode which reduces complexity of the analysis.

Cascaded Boost/Buck ERSC Operation

The ideal cascaded boost/buck ERSC, depicted in Fig. 7, has three state variables: inductor current of the effective current source, voltage across the energy buffer capacitor and current in the feedback inductor. Unlike single-ended topologies, the cascaded topologies have four active switch states which control energy storage in the feedback and buffer elements as well as in the filter element associated with an effective input



Ideal Cascaded Boost/Buck ERSC

Fig. 7 Ideal Cascaded Boost/Buck ERSC

source. All four switching states are presented in Table 4 along with state equations.

Three modes of operation are investigated for the ERSC. The modes allow for controlled energy storage in each of the three elements. The first mode is Soft-Start which controls the build-up of current, i_1, in the input filter inductor and voltage, v_C, across the buffer capacitor. The second mode is the Charge Mode which controls the charging of the buffer capacitor to a preset voltage, V_C. All input energy is transferred to the buffer capacitor during this process. When the capacitor is charged to V_C, the circuit enters the magnetize mode. This is the main mode of operation for which the circuit was designed. The feedback inductor current, i_2, increases to high current levels while i_1 and v_C are held constant within a ripple bound. All input energy is transferred to the feedback inductor in this mode.

Soft-Start Mode: This mode begins in state A of Table 4 when i_1 and i_2 equal zero, and v_C is equal to or greater than the input voltage, V_S. The switch, S_1, is modulated to build current, i_1, in the input filter inductor, L_1,

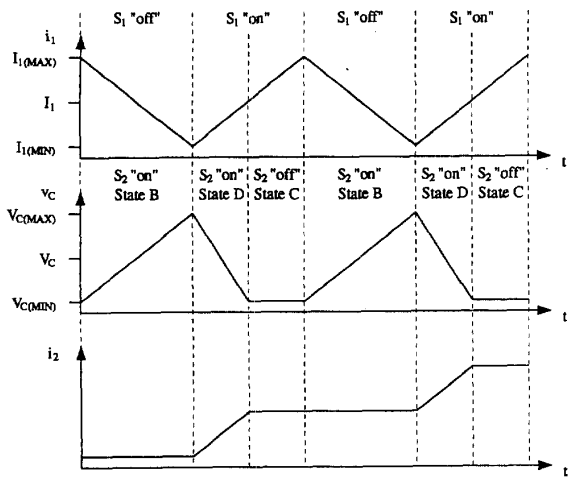


Fig. 8. Switching Sequence of Cascaded Boost/Buck ERSC in Magnetize Mode

while S_2 remains "off" keeping i_2 equal to zero. The switching of S_1 ratchets i_1 to its maximum average value, I_1 as shown in Fig. 8. The rate at which i_1 increases is varied by controlling the duty cycle of S_1 as in traditional boost converter operation. The mode ends when I_1 is reached. The $I_{1(MAX)}$ in Fig. 8 represents the maximum available current from the real (current-limited) voltage source.

Charge Mode: When i_1 reaches I_1 the circuit enters the charge mode to charge the buffer capacitor to a user-defined value, V_C, assuming V_C has not been attained during the soft-start mode. Charging of the capacitor is accomplished through current-injection control to modulate S_1. The switching of S_1 will hold i_1 at an average value, I_1, within a ripple bound between $I_{1(MAX)}$ and $I_{1(MIN)}$. Switch S_2 will remain "off" during this process to again keep i_2 equal to zero. This switching cycle will continue until v_C equals V_C.

Magnetize Mode: This is the primary mode of operation when the feedback inductor current is being charged from zero to a high value. This is accomplished by using current injection control to modulate S_1 and through modulation of S_2 to keep the voltage across the buffer capacitor between upper and lower ripple values, $V_{C(MAX)}$ and $V_{C(MIN)}$, where $(V_{C(MAX)} + V_{C(MIN)})/2$ is equal to V_C.

Switching states for the magnetize mode are shown in Fig. 8. Switch

Table 1. Cascaded Boost/Buck ERSC Switch-State Topologies

Switch-State Topologies	State Equations
State A S_1 "off" S_2 "off"	$\frac{di_1}{dt} = (\frac{1}{L_1})(V_S - v_C)$ $\frac{dv_C}{dt} = (\frac{1}{C})(i_1 + i_2)$ $\frac{di_2}{dt} = (\frac{1}{L_2})(-v_C)$
State B S_1 "off" S_2 "on"	$\frac{di_1}{dt} = (\frac{1}{L_1})(V_S - v_C)$ $\frac{dv_C}{dt} = (\frac{1}{C})(i_1)$ $\frac{di_2}{dt} = 0$
State C S_1 "on" S_2 "off"	$\frac{di_1}{dt} = (\frac{1}{L_1})(V_S)$ $\frac{dv_C}{dt} = 0$ $\frac{di_2}{dt} = 0$
State D S_1 "on" S_2 "on"	$\frac{di_1}{dt} = (\frac{1}{L_1})(V_S)$ $\frac{dv_C}{dt} = (\frac{1}{C})(-i_2)$ $\frac{di_2}{dt} = (\frac{1}{L_2})(v_C)$

S_1 is modulated independently of S_2 to hold i_1 between the specified ripple boundaries using the same current injection control technique as previously explained for the charge mode. The modulation of S_2, to hold v_C between the specified upper and lower ripple boundaries, is complex and is dependent upon both the state of S_1 and the value of V_C as shown in Fig. 8.

Cascaded Boost/Buck ERSC Analysis

All design equations are derived for the magnetize mode. To determine the duty cycle of S_1, D_{S1}, the constant change in input current, $\Delta I_1 = I_{1(MAX)} - I_{1(MIN)}$, is substituted into the state B and state D (or C) equations for the S_1 switching cycle and results in

$$t_{on(S1)} = (\Delta I_1 L_1)/ V_S \quad (1)$$

and

$$t_{off(S1)} = (\Delta I_1 L_1)/ (V_S - V_S) \quad (2)$$

Combining (1) and (2) for duty cycle yields

$$D_{S1} = (V_C - V_S) / V_C \quad (3)$$

Rearranging (3) provides an equation to determine what the buffer capacitor should charge to in the charge mode. The equation for V_C is

$$V_C = V_S / (1 - D_{S1}), \text{ a boost transfer function} \quad (4)$$

If a maximum switching frequency f_{S1} is specified for S_1 in the magnetize mode, the input filter inductance can be calculated by adding equations (1) and (2) and then solving for L_1:

$$L_1 = [T_{S1} V_S (V_C - V_S)] / (V_C \Delta I_1) \quad (5)$$

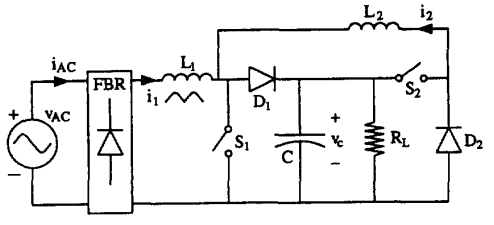


Fig. 9. Ideal Cascaded Boost/Buck PFC-ERSC

To derive an equation for the buffer capacitance state B is used. The buffer capacitance must be sized to allow v_C to increase from $V_{C(MIN)}$ to $V_{C(MAX)}$ during the constant "off" time of S1, $t_{off(S1)}$. If the change in v_C, $\Delta V_C (= V_{C(MAX)} - V_{C(MIN)})$, during state B is substituted into the voltage state equation of state B and $t_{off(S1)}$ is substituted for dt in (2), then

$$C = [I_1 \Delta I_1 L_1] / [\Delta V_C (V_C - V_S)] \quad (6)$$

where I_1 is the average value of i_1 during state B.

In the magnetize mode all energy injected from the voltage source is stored in the feedback inductor. The total input energy can be calculated by integrating the average input power across the operating period of the magnetize mode. The total input energy,
can then be equated to the energy stored in the feedback inductor when i_2 has increased from zero to a specified maximum amount, $I_{2(MAX)}$, at the end of the magnetize mode. The resulting equation is solved for L_2 if a time duration, t_m, is specified to achieve maximum current. Hence,

$$L_2 = (2 V_S I_1 t_m) / (I_{2(MAX)})^2 \quad (7)$$

It should be noted that the duty cycle of S_2, D_{S2}, is dynamic during the magnetize mode. Initially D_{S2} equals 1 for lower current values of i_2 and the circuit never enters state C. As i_2 increases to higher values, D_{S2} approaches 0.5 and S_2 switches out of phase with S_1 as the time in state D decreases. Consequently, the time in state C increases. If the circuit has parasitic losses, i_2 would stop increasing when the average input power equals the losses of the circuit. This special case of the magnetize mode, where all state variables remain constant within given ac ripple bounds, is named the *recirculate* mode.

APPLICATIONS OF ERSC

Many applications of the ERSC exist. The original application was for in-situ testing of power devices [1, 5] and is the topic of a future paper. The development shows how power devices can be tested at very high power conversion levels in the topology of their final application when only a low-power source is used as the input to the circuit.

A second application examined in detail in [5] and reviewed here involves the use of a Cascaded Boost/Buck ERSC as a novel power factor correction circuit. Precisely regulated DC output voltages are generated by the *Cascaded Boost/Buck Power Factor Correcting ERSC*. This approach can be extended to resonant topologies by substitution of the quasi-resonant switch [5,6].

Power Factor Correction

Conventional off-line switchmode supplies draw pulsating ac line current, resulting in low power factor and high rms current. To alleviate these problems, active unity power factor correction (PFC) circuits have been proposed [11, 12] which comprise a dc/dc boost converter following a bridge rectifier. The output of a boost PFC circuit can be regulated by the use of a large filter capacitor or by cascading with another regulating switchmode power converter. Either way power density is decreased through the addition of filter capacitors. Parallel PFC circuits have been introduced which consist of two switchmode power converters placed in parallel between the bridge rectifier and output to precisely regulate power flow [11.12]. Energy is stored in a capacitor in one of the switchmode converters when the input power exceeds the output power and released when the power load demand is greater than the available input power.

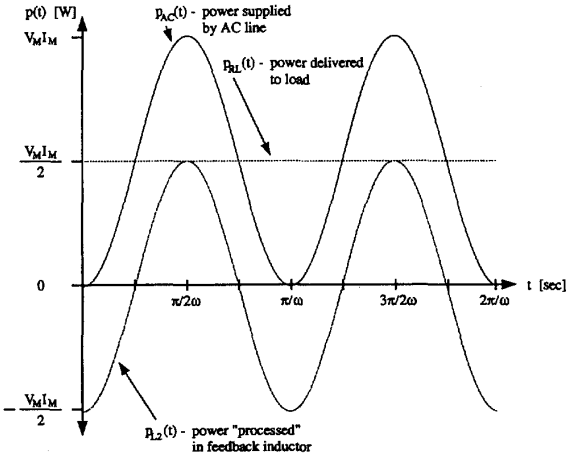


Fig. 10. Instantaneous Powers for Cascaded Boost/Buck PFC-ERSC

The Cascaded Boost/Buck ERSC can be utilized as a regulated output PFC circuit, similar to [11, 12], if the dc load is placed across the energy buffer capacitor of the ERSC. It should be noted that the DC output voltage must be higher than the peak voltage of the input source for proper boost converter operation.

PFC-ERSC Analysis

The ideal cascaded boost/buck PFC-ERSC is presented in Fig. 9. The buck portion of the circuit is used to filter the power flow to the load, R_L, by storing energy in L_2. The storage in L_2 eliminates the need for a large value of filter capacitance, C. Since this precisely regulated PFC scheme is accomplished magnetically and at high frequencies, very high power density can be realized.

To achieve a precisely regulated output voltage without generation of undesirable harmonics, switch S_1 operates independently of S_2 to sinusoidally shape the input current while controlling the amount of input power. Control techniques such as peak current-mode control, average current-mode control, and variable hysteretic control, described in [11, 12], are suitable for controlling S_1.

If the buffer capacitor voltage, V_C, is precisely regulated, and the input voltage and current are controlled to be in phase, then, for an ideal circuit the output power in load, R_L, and the input power can be related as

$$p_O(t) = V_C^2 / R_L = p_{O(AVE)} = V_M I_M / 2 \quad (8)$$

assuming the input power is

$$P_{AC}(t) = (V_M I_M / 2)\,[1 - \cos(2\omega t)] \quad (9)$$

where V_M is peak of the ac input voltage;
I_M is peak of the ac input current; and
ω is the line frequency.

Equation (8) can be rearranged to give a control equation for determining I_M as a function of $p_O(t)$ and V_M that can be used in conjunction with the before-mentioned control techniques for the modulation of S_1. The equation is

$$I_M = 2 V_C^2 / (V_M R_L) \quad (10)$$

Switch, S_2, is modulated to control the release and storage of energy in the feedback inductor to augment the source and to hold v_C relatively constant as the instantaneous input power fluctuates. A control equation for the feedback inductor current is obtained through analysis of the instantaneous power in the inductor, $p_{L2}(t)$. Subtracting (8) from (9) results in the equation for the required power "processed" in the feedback inductor L_2 as

$$p_{L2}(t) = -(V_M I_M / 2) \cos(2\omega t) \quad (11)$$

The circuit is simulated in [5] and the comparison of (8), (9) and (11) are given in Fig. 10. The power flow through the feedback inductor controlled by S_2 is sinusoidal indicating no net build-up of energy during steady-state operation. An expression describing the inductor current, is obtained by integrating (11) to give the instantaneous energy stored in L_2. Equating energy to $[L_2 i_2^2(t)]/2$ gives

$$i_2(t) = (\beta_1 \sin(2wt) + \beta 2)^{1/2} \quad (12)$$

where $\beta_1 = -V_M I_M / 2\,\omega L_2$
$\beta_2 = 2K / L_2$ and
K is constrained by, $i_2(t) \geq 0$ giving
$K \geq V_M I_M / 4\,\omega$

Note the control of S_2 is quite complex.

Summary

A new class of power circuit topologies, which allow for controlled energy recirculation and storage, has been established and are herein named Energy Recirculation and Storage Circuits (ERSCs). These are derived from port reductions of dc/dc switchmode power converters by removing the load from a converter and connecting output to input to form a recirculation and storage path. Formal port-reduction rules are established for constant-current- and constant-voltage-port, ladder-structured converters which exhibit a common connection between the input and output terminals of like polarity. The port reduction rules are utilized to derive a family of ERSCs from six basic pwm dc/dc switchmode power converter topologies. A cascaded boost/buck ERSC is analyzed to show proof of concept and provide an example of ERSC operation. Two applications are cited for the ERSCs. The first involves the use of ERSCs for in-situ testing of power devices. Devices can be exposed to the naturally occurring electrical stresses of their final application at power levels well in excess of the source capabilities. A second application uses a cascaded boost/buck ERSC for power factor correction and is analyzed in detail. The feedback of stored energy allows augmentation of the source to keep the power factor near unity.

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