A Framework for Developing Power Electronics Packaging

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Abstract - As the integration of electro-physical circuits increases, many physical components and topologies are either directly or indirectly determined by the electrical designer. This paper presents a packaging technology framework for designers to better understand, evaluate and communicate the technical needs for a 'physical circuit'. The framework goes further in proposing a systematic method to link technical power packaging issues to user requirements as the basis for developing a Power Electronics Technology Roadmap.

This paper presents the framework as a three-dimensional coordinate of User Requirements, Levels of Packaging, and Interfaces and Pathways, cross-cut by a fourth dimension of Energy Forms. Examples assist the reader in understanding the framework and appreciating the potential for application of the framework in the future developments of power electronics packaging.

I. INTRODUCTION

A continual endeavor in power electronics is to increase power density. During the last two decades circuit frequencies have increased, thus, requiring smaller dimensions to allow for the higher frequencies. The electrical and physical interaction has become so great that there no longer can be a separation between the electrical and physical design functions.

Power electronic circuits condition or convert a multitude of energies, such as electric, magnetic, mechanical and thermal. It is, therefore, unreasonable that design of a power electronic circuit be considered solely as an electrical design. An integrated, electro-physical approach should be used. However, the core of a power electronic system is, and will remain, electrical energy, even though other energy forms for sensing, actuation and isolation are included. Thus, the electrical designer will be the designer of choice for the future and will evolve with physical design becoming part of her (or his) knowledge base. (This is well underway. The power electronics designer is well versed in thermal issues to the extent that he (or she) can lead or directly perform thermal design.)

To evolve this knowledge base a *packaging technology framework*, Fig. 1, should be put in place that all designers can use to understand the commonality and duality of electrical and physical design. The framework shows a logical progression from technical *user requirements* to the 'hard-core' technical issues in packaging.

It is equally important that the power electronics industry evolve in integrating electrical and physical systems. To guide the industry, a power electronics packaging roadmap is needed. To systematically and comprehensively develop the packaging roadmap a *packaging technology framework* is also needed. The same framework applies to the evolution of the designer as to the evolution of the industry.

The *packaging technology framework* has a number of uses. First, it systematically establishes present design, technology and user profiles. Secondly, it provides a comprehensive checklist of all technical issues as a vehicle to predicting future packaging trends - a roadmap. Lastly, it is a tool to allow designers to have insight into the interrelationships of packaging, thus, resulting in better optimized system packaging designs.

The *packaging technology framework* will provide a systematic method to link technical packaging issues to *User requirements*. This is the first proposal of a technical, systematic approach to defining a packaging roadmap.

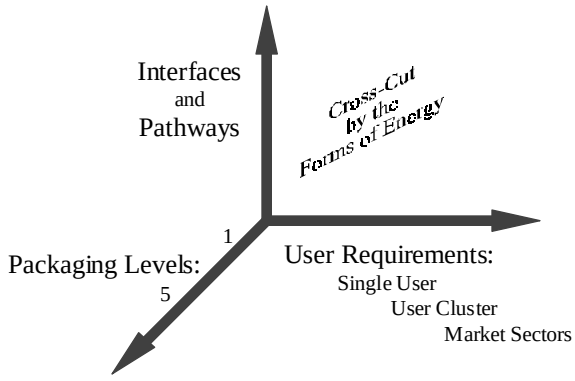

Figure 1. Framework for Power Electronic Packaging Technology.

This paper will describe the various elements of the technology framework for power electronics packaging. It will present each of the axes shown in Fig. 1 and provide examples that will assist the reader in understanding the framework and appreciating the potential for application of the framework in the future developments of power electronics packaging.

II. PACKAGING ROADMAP UPDATE

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At the APEC 1997 conference and exhibition in Atlanta, GA, February 23-27, 1997, a meeting of the PSMA Board of Directors proposed that a technology roadmap for Power Electronic Packaging should be produced which would define industry concerns in power electronic packaging. Such an initiative should allow the identification of deficiencies in existing knowledge, materials and components, which could be addressed, in a coordinated manner, through industry or government initiatives.

A parallel initiative was also proposed which would report on the state-of-the-art in power electronic packaging with the objective of defining a starting point/benchmark for the technology roadmap as shown in Figure 2. The authors of this paper are currently involved in the development a State Of the Art Review in Power Electronic Packaging, SOARPEP [1]. This starting point will integrate with the evolving technology drivers in power electronics to provide an ongoing direction for development of the industry.

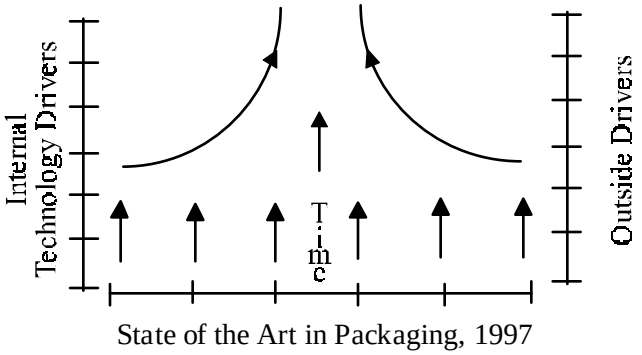

Figure 2. Power packaging roadmap approach.

SOARPEP proposes to base its report on the *packaging technology framework* which is presented in this paper, thereby providing the first demonstration of the application of the framework in the analysis of power electronic packaging. SOARPEP is being run by a steering committee consisting of Dr. O Mathuna, Mr. Flannery and Mr. Alderman (with addresses noted in the heading). The secretariat for the initiative is provided by PEI Technologies, National Microelectronics Research Centre, University College, Cork, Ireland. A committee of contributors has been drawn from industry and academia to provide inputs to the initiative. Details of the SOARPEP initiative are available from PEI Technologies at NMRC at e-mail address pei@nmrc.ucc.ie.

The review focuses on current state-of-the-art in commercial products using public domain information obtained from committee members. This includes information from committee members' experience, product specifications, market surveys and trade journals. The review also covers information available in published technical literature including peer reviewed technical journals and technical conference proceedings.

Volunteers are welcome to join in the SOARPEP and road mapping activities. The breadth and complexity of the activities requires a large number of volunteers to research and formulate a technology projection. Contact the authors for more information.

III. DEFINING PACKAGING

The viewpoint in a power electronics design that 'if it is physical, it is packaging' lumps all non-electrical issues into one area and makes the understanding, evaluation and development of packaging designs difficult. The initial steps, then, must be to define packaging, delineate the areas of electro-physical design, and provide a set of common boundaries and terms for clear common understanding.

> *"Packaging is the arranging of physical components to provide a function or characteristic that is compatible with external interfacing elements."*

This is the essence of *physical circuit* design. Manufacturing embodies the *processes* to fabricate that arrangement. Although packaging and manufacturing are strongly interrelated, they are not synonymous. (The IEEE Components, Packaging and Manufacturing Technology Society clearly delineates a difference just by its name.)

To better understand the correlation between electrical and physical circuits (and systems), consider the morphology of a generic circuit. A circuit has three partitions: components, topologies and controls. The components are active or passive. The topologies are the positioning of the components to provide a function. The *controls* provide a preferred set of rules for operation of those components. It is obvious to the power electronics designer how the domains apply to electric circuits.

Physical circuits have the same domains: *components*, such as heat sinks and PCBs (printed circuit boards); the *topologies*, such as the stack structure of silicon soldered on copper on ceramic; and, finally, controls (which is not as prevalent) can be found in thermo-electric coolers and active fluid cooling systems. Most of the interest in physical circuits lies with components and topologies.

To better define "physical," one should first define "electrical". "Electrical" identifies the form of energy being processed. Hence, "physical" represents the other forms of processed energies, such as mechanical, thermal, chemical, photonic, etc. This paper will limit the discussion to four energy forms: electric, magnetic, mechanical and thermal. (Not included are secondary forms such as acoustic.)

A common phrase to power electronics designers is the "… circuit," such as a "magnetic circuit". The phrase indicates a topology for processing magnetic energy. In education, equivalent electrical topologies are used to model thermal circuits. Hence, it can be concluded that

An electro-physical 'circuit' defines the circuits of multiple energy forms. All energy forms have components and all have optimum topologies to create a specified function.

The foremost concern in power electronics continues to be the efficient processing of energy. Unlike the computer and telecom areas which process "information," the power electronics area processes energy. Therefore, use of energy as a foundation in the development of the *packaging technology framework* should be expected.

An example of a packaging problem relating the four energy forms of interest is: a high frequency magnetic core couples the radiated field into a copper conductor on a PCB. This causes eddy current heating and increasing the skin-effect resistance. Higher resistance loss further increases conductor heating which increases the mechanical stresses between the conductor and PCB leading to early failure. [Who would notice the problem first: The electrical designer through circuit loss measurements; The thermal designer through a thermograph of that specific spot, or the packaging engineer who first notices the conductors are lifting off the board and assumes the conductor adhesion is poor because of faulty chemistry?]

IV. THE PACKAGING TECHNOLOGY FRAMEWORK

The proposed framework is a four-dimensional matrix of

- *user requirements,*
- *levels of packaging,*
- *interfaces and pathways, and*
- *the four forms of energy.*

Figure 1 graphically shows the first three dimensions as axes which are then cross cut by the four energy forms. The three axes are discussed below.

User requirements

The *user requirements* provide the technical specifications that reflect internal industry technology drivers. These are determined through divisions industries and products.

The task of dividing industries and determining drivers begins at either the individual user or the market sector (users clustered by common application) as diagrammed in Figure 3. These clusters (market sectors) are methodically grouped and identified by the equipment and component suppliers in order to establish as large a user base as possible. Requirements derived from the user cluster, as opposed to the individual user, have a much higher impact on equipment design simply from their combined impact and thus become industry drivers.

Looking at requirements by the potential for impact from the "bottom up" provides a sequential list:

Individual User – a single design - impacts design;
Small user Cluster – a single application - impacts common design solutions, some use of unique approaches;
Large User Cluster – an industry application - impacts technology, designs, components, and the supporting infrastructure (e.g. pick and place equipment for surface mount technology).

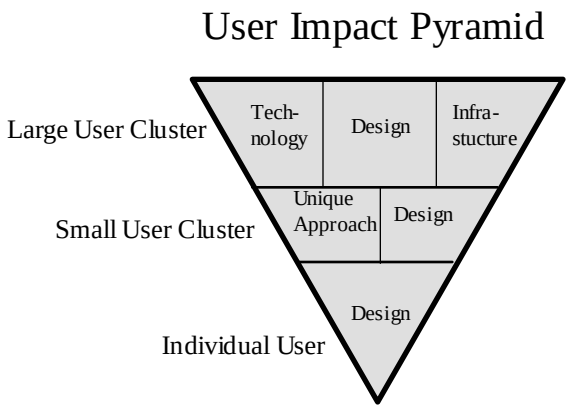

Figure 3. User focus as technology driver.

Continuing with the "bottom up" view of impact, the technologies are driven by single, high volume users (a telecom company) or by high performance demand applications (space satellites). Here, the demands that cannot be served by existing approaches drives new technologies and designs.

Thus a road mapping task involves the following concept equation

$$\textit{Resulting Technology Direction} = \alpha * \textit{User Cluster Requirements Drivers} + \beta * \textit{High Performance Requirement Drivers}$$

where α and β are the impact factor of the user and performance requirement on considered technologies.

The high performance requirements drivers are identified by individual-user programs and the technologies developed to serve them. Often these technologies are outside the boundary of general-user requirements — most often that boundary is cost. However, these are very important in roadmap generation as they lead general technology and will possibly be utilized to satisfy some user cluster requirements.

To address the user cluster requirements, Who, What, When must be asked. The procedure is:

1) identify the clusters or market sectors appropriate to the power supply supplier industry [who]
2) identify the clustered present requirements [what] and

3) identify the requirement trends for those clustered requirements [when]

Examples of large user clusters for power supply equipment are given in Table I.

Table I. Examples of Large User-Cluster for Power Supply Equipment

Sector	Portables		Mid-Range		High-End	
	AC	DC	AC	DC	AC	DC
Computer	ac adapter	battery charger	200W ac/dc PwrSup	none	6000W ac/dc Conv.	1500W dc/dc PwrSup
Automotive	none	mobile telephone charger	none	auto radio PS	electric vehicle charger	electric power system boost converter
Consumer Brown Goods	walkman power supply		Cable TV settop PS	marine TV supply	projection TV supply	
Consumer-White Goods			washer control supply	marine refrigerator	microwave oven PS	
Gov./Space		battery operated surveillance equipment supply	field radio supply	submarine aux. equipment supply		Satellite PS
Industrial		portable bar code scanner supply		24V/5V panel supply	plating supply	
Medical/ Instru.	home apnea monitor supply	pacemaker supply	heart bed side monitor PS	defibrillator PS	MRI PS	
Office Automation	ink jet printer supply	ink jet battery supply	laser printer PS		large copier PS	
Telecom	home phone PS	SLIC supply		board mounted power module	remote site 2kW supply	
Networking	LAN terminal supply		small server supply		network switcher PS	

The categories are aligned with the PSMA Roadmap "Power in the Year 2000" [[2]]. Portable is <25W, Mid-range is 25W to 300W and High-end is >300W.

The *user requirements* are also cross-cut according to the different energy forms, i.e.

- electrical requirements,
- magnetic requirements (EMI regulations),
- mechanical constraints,
- thermal requirements,

or global requirements beyond power processing, such as

- control interfacing requirements and monitoring,
- and more recently, the environmental impact ("green" issues).

These requirements are physical in nature and associated with different energies (e.g. chemical, electrical, magnetic, mechanical and thermal). Relating the requirements to all relevant energy forms provides a comprehensive and unifying approach to a *packaging technology framework* never before proposed.

Levels of Packaging

The *Levels of Packaging* is another axis in the roadmap evaluation matrix. The intent here is to divide a system, top-down, into lower and lower subassemblies with the boundary drawn between assembly and subassemblies shown in Fig. 4. Requirements, trends, and the roadmap are developed at each level based on

1) The boundary conditions of electrical / mechanical / thermal performance characteristics within the level.
2) The electrical / mechanical / thermal interconnection between each level.

Each level is defined and numbered, bottom-up, in a micro to macro manner. There are five traditional levels in electronic packaging [3] also applicable to power packaging. Note that Levels are not easily defined. Some packages may be categorized in either of two levels depending on the application.

Level-1: Component(s) in Package. This is basic component packaging. Examples include mount-down and lead attach of a component or semiconductor in a discrete package, or multiple components in a module. Traditional 'chip and wire' hybrid circuits mounted in a housing (often hermetic) are Level-1 packages. The package provides a 'self contained environment' that allows the components to be tested, transported and used at the next higher level of packaging while buffering electrical, mechanical and chemical discontinuities from the next level. This package becomes a subassembly to the next higher level.

Level-2: Package on Board. These boards carry mixed-technology components (capacitors, resistors, inductors and packaged discretes) that are usually coated and terminated with a connector. Examples are PCB, IMS (insulated metal substrate) and SMT boards. They differ from Level-1 in the lesser sophistication in fabrication. The board provides a functional partition and is a subassembly to the next packaging level.

Level-1.5 *(half-level):* Chip on Board (COB). This mounts 'chip and wire' semiconductors directly to a PCB or on IMS. A driver in packaging is to combine levels. An objective of the road map will be the development of a direction to combine levels.

Level-3: Board in Rack or Sub-Assembly Level. At this level the rack or case is considered. Each board or module is a subassembly with a back connector interfacing to the rack backplane connectors. Another example is the sub-modules in a power supply such as the output module sub-assembly where there might be several for a multi-output power supply or the PFC module sub-assembly. Each of these sub-assembles connect to the overall power supply main assembly. The sub-module approach is being utilized where flexibility and fast assembly time are both required to serve a certain market.

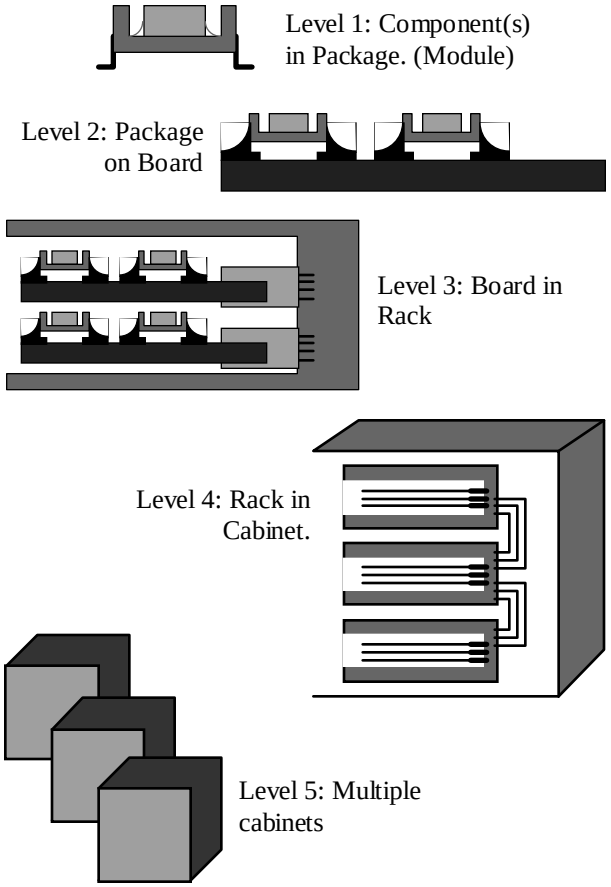

Figure 4. Levels of packaging.

Level-4: Rack in Cabinet or Sub-Cabinet Level. A single cabinet is sub-divided for assembly purposes. A rack is a common cabinet sub-division. Functional assemblies with common dimensions are stacked the full cabinet width. In this arrangement, common signals and power bussing can be routed quite easily.

Level-5: Cabinet in Room or Multiple Cabinet Level. Here the entire cabinet is considered. Usually requires floor space availability and compatibility with adjoining cabinets, room interconnect facilities, and allowable room ambient conditions that include impact on operator interference (sound, heat, etc.). At this level, the power supply is usually a sub-assembly within the cabinet or is perhaps a rack level component serving a restricted section of the cabinet. Many system designs end at this level as the system is self contained in a single cabinet.

Producers and suppliers have business thrusts that are aligned along one or more packaging levels. Note, that combining levels, as done with Levels 1 and 2, is of great advantage.

Interfaces and Pathways (I&P)

The last dimension completes the formulation of the very fundamental technical issues to be pursued in the packaging roadmap or by the designer. All technical issues in packaging can be reduced to issues of either the interface to or the pathway for the flow of energy. This is comprehensive in that it represents the inter-connection and intra-connection, within and between levels.

Applying I&P to the different Levels of Packaging is straight forward. Assuming that the characteristics of a component or sub-assembly from the next lower packaging level are established, the issues pertinent to the flow of energy are then sought. Specifically, the interfacial issues are sought related to the mounting or assimilation of the component or sub-assembly into the Level of interest, and the pathway issues for energy conduction relating to the board or housing of that Level. For each level then,

The interface issues are of the chip in a package and the pathway issues of energy flow through the package.
The interface issues are of the package on the board and the pathway issues of energy flow through the board.
The interface issues are of the board placed into a rack and the pathway issues of energy flow through the rack.
The interface issues are of the rack placed in a cabinet and the pathway issues of the energy flow through the cabinet.
The interface issues are of the cabinet placed among others or in a room and the pathway of energy flow among the cabinets and through the room.

Again, the forms of energy cross-cut both the I&P and Levels. An example of thermal issues would address the flow of heat from a chip package through the solder attach interface, and then the conduction and spreading through the board. Also, electrical and mechanical issues arise.

Several examples will clarify the concept. Note, that the power electronics designer apply the following procedures to

future designs. The procedures are most applicable to design teams.

A connector will be used as an example Level 1 component for evaluation. The Example 1 lists example issues for each of the energy forms as it pertains to the interface or pathway of the connector.

Example 1. Level-1 Issues Relating to a Connector

I&P	ISSUES
Interface (to the chip)	
Electrical	sufficient wiping action to maintain low resistance contact
Magnetic	is it a shield to limit EMI radiation
Mechanical	contact force
Thermal	surface area of leaf for conduction, need special design
Pathway (through the package)	
Electrical	conductivity of copper clad versus BeCu metal leafs
Magnetic	ferromagnetic metals causes higher connector inductance
Mechanical	translation of force from insertion of a card on one side stresses the solder connection on the other
Thermal	thick metal helps to conduct heat through connector

A second example is a Level-2 package hosting a 200W, 5V ac/dc mid-range power supply. A sampling of the issues are given in Example 2.

Example 2. Level-2 Issues Relating to a Power Supply

I&P	ISSUES
Interface (to the component)	
Electrical	solder impedance of components
Magnetic	proximity of associated components
Mechanical	component adhesion
Thermal	Heat sink attach
Pathway (through the board)	
Electrical	copper trace resistance on the board
Magnetic	lead and trace inductance
Mechanical	rigidity and lead vibration suppression
Thermal	maximum hot spot temperature, and board aerodynamics

The third example, given in Example 3, cites issues of placing multiple boards in a rack. Hot-swap issues would be identified by applying the procedure to a host of operational circumstances.

Listed in Examples 1 -3 are issues of relevant concern. The final step in utilizing the framework is to identify the action to be taken by relating the issues to the *User Requirements*. For example, a strategic positioning of fans in a rack housing (Level-4) with the properly adjusted air flow will be able to meet the *User Requirements* for a certain *maximum temperature* and provide a certain *thermal density* in the housing. As early stated, the previous level "sub-assembly" characteristics are assumed to be known. In this case the heat generation of the boards should be known by the board designers and passed on to the assemblers.

Example 3. Level-3 Issues Relating to Rack Mount Supply

I&P	ISSUES
Interface (to the boards)	
Electrical	connector resistance
Magnetic	board cross-coupling noise
Mechanical	rigidity of guide slides
Thermal	cold plate attach
Pathway (through the rack)	
Electrical	back plane wiring resistance
Magnetic	EMI shielding
Mechanical	vibration
Thermal	rack aerodynamics

V. ROAD MAPPING AND THE TECHNOLOGY DRIVERS

The fan and housing example above illustrate the application of the framework to a packaging technology roadmap. If the User requirements noted above cannot be met with present technology, do the fans become the focus for technological innovation? Do the boards?… Components? All of the above? The framework will allow a systematic quantification of issues relevant to the thermal challenges at all levels of packaging.

In this case, innovation could be sought for the highest leveraging solution within one of the levels. This would be one obvious roadway. Another roadway would be to use advanced technology to combine levels. This is the continual move toward integration. A third roadway would cross-couple energy forms, i.e. decrease the problems occurring in one energy form by making changes in another form.

As the roadmap develops, hopefully, many roadways will become event which have yet to be considered. Once the roadways are identified and given a timeline and cost, it will be the industry's responsibility to determine the direction of the journey to evolve the *power electronics packaging technology*.

SUMMARY

A *packaging technology framework* is described that offers a systematic method to link technical packaging issues to *User requirements*. The framework has a number of uses. First it systematically establishes present design, technology and user profiles. Secondly, it provides a comprehensive checklist of all technical issues as a vehicle to predict future packaging trends - a roadmap. Lastly, it is a tool to allow designers insight into the interrelationships of packaging, thus, resulting in better optimized system-packaging designs. This is the first proposal of a technical, systematic approach to defining a packaging roadmap.

The framework is divided into a three-dimensional coordinate of User Requirements, Levels of Packaging, and Interfaces and Pathways, cross-cut by a fourth dimension of Energy Forms. The User Requirements are derived from user

clusters which are classified by the impact they have on technology drivers. The Levels of Packaging follow established divisions in telecom and computer electronic packaging, but are extended to five levels which traverse chip-in-package to multiple cabinets in a room.

All levels share having components or subassemblies that are formed into circuits or topologies. The topologies provide pathways to the flow of electric, magnetic, mechanical and thermal energies. However, there are impediments along the pathways and at interfaces. The last axis in the framework offers a systematic method to identify the issues related to the energy flows along the Interfaces and Pathways.

Examples assist the reader to apply the framework in the development of power electronic designs. Further, the reader is offered insights into the potential for development of a *power electronics packaging roadmap*. Once roadways are identified, industry can, then, determine the direction of the journey to evolve the *power electronics packaging technology*.

REFERENCES

[1] S. C. Ó Mathúna, et. al., "State of the Art Review of Power Electronics Packaging (SOARPEEP)," report in progress.

[2] D. Staffiere and J. Sarjeant, ed., "The Power Technology Roadmap Report," Power Sources Manufacturers Association, 14 Ridgedale Ave., Suite 125, Cedar Knolls, NJ 07927, PSMA@PSMA.Com.

[3] R. R. Tummala and E. J. Rymaszewski, Microelectronics Packaging Handbook, Van Nostrand Reinhold, New York, 1989.