A Four-Dimensional Road-Mapping Framework for Power Packaging Technology

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Abstract - This paper proposes a systematic method to link technical power packaging issues to user requirements as the basis for developing a Power Electronics Technology Roadmap. The framework goes further in proposing a framework for designers to better understand, evaluate and communicate the technical needs for integration of electro-physical power electronic circuits.

This paper presents the framework as a three-dimensional coordinate of User Requirements, Levels of Packaging, and Technical Issues, cross-cut by Forms of Energy. Examples assist the reader in understanding the framework and appreciating the potential for application of the framework in the future developments of power electronics packaging.

Introduction

The foremost concern in power electronics continues to be the efficient processing of energy. Unlike the computer and telecom areas which process "information," the power electronics area processes energy. Therefore, use of energy as a foundation in the development of the *packaging technology framework* should be expected.

Also, the continual endeavor in power electronics is to increase power density through smaller dimensions to allow for the higher frequencies. The electrical and physical interaction has become so great that there no longer can be a separation between the electrical and physical design functions, but a common *electro-physical* approach.

The "electrical" in *electro-physical* identifies the form of energy being processed. "Physical" represents the other forms, such as mechanical, thermal, chemical, photonic, etc. This paper will limit the discussion to four energy forms: electric, magnetic, mechanical and thermal. Technologies in all basic energies need to be developed to technically support the evolution of power electronic systems.

To guide the technology developments and the industry evolution, a *power electronics packaging roadmap* is needed. To systematically and comprehensively develop this roadmap a *Packaging Technology Framework* is needed.

This paper will describe the various elements of a technology framework for power electronics packaging. It will present each of the axes shown in Fig. 1 and provide examples that will assist the reader in understanding the framework and appreciating the potential for application of the framework in the future developments of power electronics packaging.

The Packaging Technology Framework

The proposed framework is a four-dimensional matrix of

- User Requirements,
- Levels of Packaging and
- Technical Issues, cross-cut by
- the four Forms of Energy,

and can be used to

- provide a comprehensive checklist of all technical issues as a vehicle to predicting future packaging trends, systematically establish benchmarks in present designs, technology and user profiles.

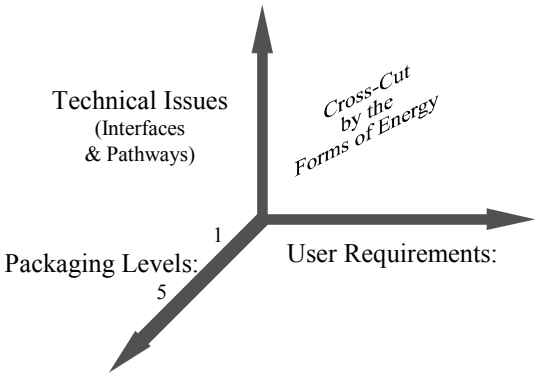

Figure 1. Framework for Power Electronic Packaging Technology.

- provide designers with insight into the interrelationships of packaging, thus, resulting in better optimized system packaging designs,

and for the development of a common knowledge base.

The foremost concern in power electronics continues to be the efficient processing of energy. Unlike the computer and telecom areas which process "information," the power electronics area processes energy. Therefore, use of energy as a foundation in the development of the *packaging technology framework* should be expected. The three axes discussed below each contain issues relating to each of the different energy forms: electric, magnetic, mechanical and thermal.

User Requirements

The *User Requirements* reflect the technology drivers for the industry and, at the lowest level, represent the technical specifications that designers use. The requirements are determined through divisions of industries and products.

The task of dividing industries and determining drivers begins with either the *individual user* or with *clustered users* (i.e. users clustered by common applications defining a *market sector*) as diagrammed in Figure 2. These clusters are methodically grouped and identified by the equipment and component suppliers in order to establish as large a user base as possible. Requirements derived from the user clusters, as opposed to the individual users, have a much higher impact and, thus, become industry drivers.

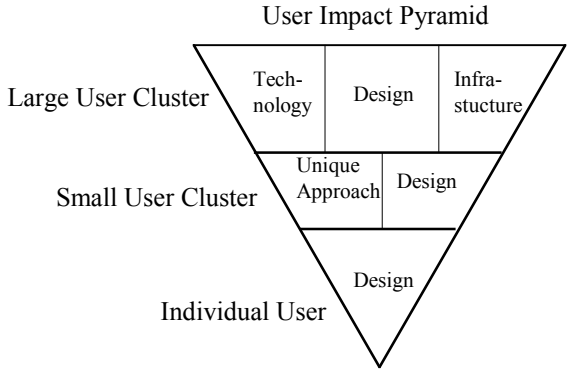

Figure 2. User focus as technology driver.

The impact of the User, and their consequential requirements, on technology can be viewed as a sequential list:

Individual User – impacts unique design approaches;
Small User Cluster – impacts designs and develop common approaches;
Large User Cluster – impacts the above, but also technology and the supporting infrastructure (e.g. pick and place equipment for surface mount technology).

Continuing with the "bottom up" view of impact, the technologies are driven by single, high volume users (a telecom company) or by high performance demand applications (space satellites). Here, the demands that cannot be served by existing approaches drives new technologies and designs.

Thus a road mapping task involves the following concept equation

Resulting Technology Direction =
α * *User Cluster Requirements (Small and Large)*
+ β * *Unique Requirements*

where α and β are the impact factor of the user and performance requirement on considered technologies.

The high performance requirements drivers are identified by individual-user programs and the technologies developed to serve them. Often these technologies are outside the boundary of general-user requirements — most often that boundary is cost. However, these are very important in roadmap generation as they lead general technology and will possibly be utilized to satisfy some user cluster requirements.

To identify user cluster requirements, a who, what, when approach can be taken, that is:

- identify the clusters or market sectors appropriate to the (power supply) supplier industry [who]
- identify the clustered present requirements [what] and
- identify the requirement trends for those clustered requirements [when]

Examples of large user clusters for power supply equipment are given in Table I. The categories are aligned with the PSMA Roadmap "Power in the Year 2000" [1]. Portable is <25W, Mid-range is 25W to 300W and High-end is >300W.

Technical specifications are derived from the *user requirements.* These are the specifications that designers directly use and can be categorized into the four energy forms, or into global requirements beyond the power processing circuits, such as

- control interfacing requirements and monitoring,

- and more recently, the environmental impact ("green" issues).

Table I. Examples of Large User-Cluster for Power Supply Equipment

Sector	Portables		Mid-Range		High-End	
	AC	DC	AC	DC	AC	DC
Computer	ac adapter	battery charger	200W ac/dc PwrSup	none	6000W ac/dc Conv.	1500W dc/dc PwrSup
Automotive	none	mobile telephone charger	none	auto radio PS	electric vehicle charger	electric power system boost converter
Consumer Brown Goods	walkman power supply		Cable TV settop PS	marine TV supply	projection TV supply	
Consumer-White Goods			washer control supply	marine refrigerator	microwave oven PS	
Gov./Space		battery operated surveillance equipment supply	field radio supply	submarine aux. equipment supply		Satellite PS
Industrial		portable bar code scanner supply		24V/5V panel supply	plating supply	
Medical/ Instru.	home apnea monitor supply	pacemaker supply	heart bed side monitor PS	defibrillator PS	MRI PS	
Office Automation	ink jet printer supply	ink jet battery supply	laser printer PS		large copier PS	
Telecom	home phone PS	SLIC supply		board mounted power module	remote site 2kW supply	
Networking	LAN terminal supply		small server supply		network switcher PS	

The *User Requirements* can be associated with different energy forms and are but one dimension of the matrix of the framework. Relating the requirements to all relevant energy forms provides a comprehensive and unifying approach to a *packaging technology framework* never before proposed.

Levels of Packaging

The *Levels of Packaging* is another axis in the roadmap matrix. The intent here is to divide a system into lower and lower assemblies with the boundary drawn between subassembly and assemblies, as shown in Fig. 3. At each level there will be a 'component' and 'carrier'. Requirements, trends, and the roadmap are developed for each level based on the

- electrical, mechanical and thermal performance characteristics *within the level*.
- electrical, mechanical and thermal interconnection *between each level*.

There are three traditional levels in microelectronic packaging [2] which are also applicable to power packaging. However, two further levels are added. None of these levels are not easily defined for some packages depending on the application.

Level-1: Component(s) in Package. This is basic component packaging. Examples include mount-down and lead attach of a component or semiconductor in a discrete package, or multiple components in a module. Traditional 'chip and wire' hybrid circuits mounted in a housing are Level-1 packages. The package provides a 'self contained environment' that allows the components to be tested, transported and used at the next higher level of packaging while buffering electrical, mechanical and chemical discontinuities from the next level. This package becomes a subassembly to the next higher level.

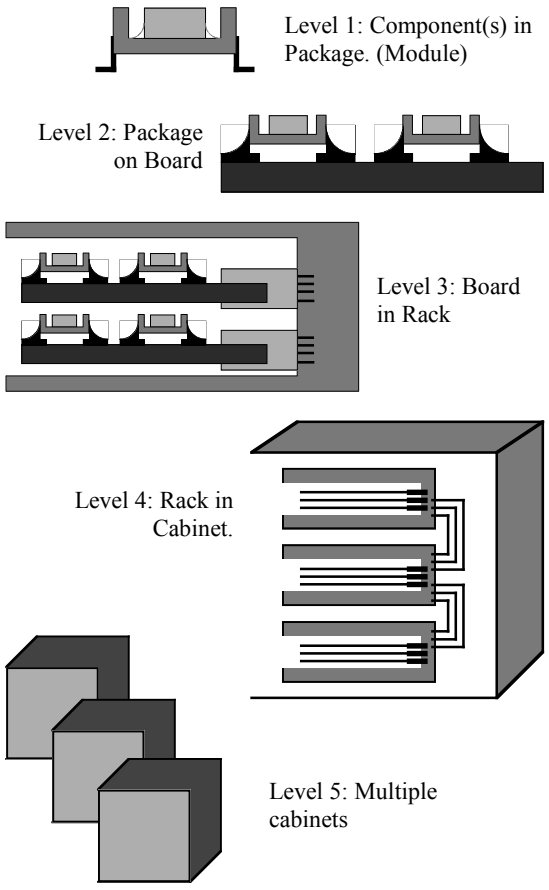

Figure 3. Levels of packaging.

Level-2: Package on Board. These boards carry mixed-technology components (capacitors, resistors, inductors and packaged discretes)

that are usually coated and terminated with a connector. Examples are PCB, IMS (insulated metal substrate) and SMT boards. They differ from Level-1 in the lesser sophistication in fabrication. The board provides a functional partition and is a subassembly to the next packaging level.

Level-1.5 *(half-level):* Chip on Board (COB). This mounts 'chip and wire' semiconductors directly to a PCB or on IMS. A goal in packaging is to combine levels. An objective of the road map will be the development of a direction to combine levels.

Level-3: Board in Rack. Each board or module is a subassembly component mounted into a rack or case. A typical example would be a board and edge connector interfacing to the rack backplane connectors. Another example is the sub-modules in a power supply such as the output module sub-assembly where there might be several for a multi-output power supply or the PFC module sub-assembly all mounted in an open frame housing.

Level-4: Rack in Cabinet or Sub-Cabinet Level. A single cabinet is sub-divided for assembly purposes. A 17.5" rack is a common cabinet sub-division. Functional assemblies with common dimensions are stacked the full cabinet width. In this arrangement, common signals and power bussing can be routed quite easily.

Level-5: Cabinet in Room or Multiple Cabinet Level. Here the entire cabinet is considered a component which requires floor real estate. Must have compatibility with adjoining cabinets, room interconnect facilities, and allowable room ambient conditions that include impact on operator interference (sound, heat, etc.).

Note, that producers and suppliers have business thrusts aligned along one or more packaging levels. Thus, this axis of a technology roadmap can be an important guide to business growth strategies. Combining levels, as done with Levels 1 and 2, is of great advantage in terms of many requirements, such as cost, reliability and manufacturability. A business can develop a niche market or gain product leverage by crossing or combining levels.

Technical Issues

The last dimension completes the formulation of the very fundamental issues to be pursued in a *Packaging Technology Roadmap* (or by a designer). All *Technical Issues* in packaging can be reduced to issues of either the '*interface to'* or the '*pathway for'* the flow of energy. Specifically, the *interfacial issues* are sought for mounting a component into the packaging Level and related to the energy flow across the interface, and the *pathway issues* sought for energy conduction relating to the carrier (or 'board') of that Level. This approach is comprehensive in that it represents the inter-connection and intra-connection, within and between Levels.

Assuming that the characteristics of a sub-assembly (or 'component') from the next lower packaging level are established, the issues about the flow of energy lead directly to the *Technical Issues*. For each level then,

The interface issues are of the chip placed in a package and the pathway issues are of energy flow through the package.

The interface issues are of the package placed on the board and the pathway issues are of energy flow through the board.

The interface issues are of the board placed in a rack and the pathway issues are of energy flow through the rack.

The interface issues are of the rack placed in a cabinet and the pathway issues are of energy flow through the cabinet.

The interface issues are of the cabinet placed among others or in a room and the pathway issues are of energy flow among the cabinets and through the room.

Again, the forms of energy cross-cut both *the Technical Issues* and *Levels of Packaging*. An example of thermal issues would address the flow of heat from a chip package through the solder attach interface, and then the conduction and spreading of heat through the board. Also, electrical and mechanical issues arise.

An energy form excluded from consideration here is chemical energy. The 'green issues' and corrosion all fall within chemical energy. Another important topic is Partial Discharge in insulation layers. This can be viewed as a chemical issue, or better, as an 'Electronic' energy issue. This contrasts 'Magnetic' energy, or in the broader view, is Electrostatic vs. Electromagnetic energy.

The framework can also be used by an electro-physical designer [3], who would use technology at hand. The framework shows the interdependencies of design issues, particularly, in the different energy forms. Designers, by education, develop expertise in one energy form, e.g. electrical designers, mechanical

designers, etc. The framework provides a common discussion platform, and allows one designer to comprehensively and systemically view the issues or concerns that need to be addressed by the others.

Road Mapping And The Technology Drivers

Examples of Technical Issues

Several examples will clarify the concept of using the framework to generate technical issues that technology must address now and in the future. The first example lists the issues for each energy form as it pertains to the interface or pathway in Level-1 chip in a package.

Example 1. Level-1 Issues for Chip on DBC

	ISSUES
Interface (chip to package)	
Electrical	resistance of source connections, wire vs. power flip-chip
Magnetic	inductance between gate contact and package pad
Mechanical	stress of Cu strap to top side of chip
Thermal	heat conductance from chip to package through solder interface
Pathway (through the package)	
Electrical	conductivity of copper clad DBC traces
Magnetic	inductance of gate and source leads for Kelvin connection
Mechanical	delimitation of Cu from ceramic
Thermal	heat spreading through package, need for spreader.

Example 2 is for a Level-2 package used in a 200W, 5V ac/dc mid-range power supply module.

Example 2. Level-2 Issues for AC/DC Circuit Board

	ISSUES
Interface (to the components)	
Electrical	solder impedance of component leads
Magnetic	proximity of associated components
Mechanical	component adhesion
Thermal	Heat sink attach
Pathway (through the board)	
Electrical	trace resistance on the board
Magnetic	trace inductance
Mechanical	rigidity and lead vibration suppression
Thermal	maximum hot spot board temperature

Example 3 cites issues of placing multiple boards in a rack. Hot-swap issues would be identified by applying the procedure to a host of operational circumstances.

Example 3. Level-3 Issues for Rack Mount Supply

	ISSUES
Interface (between boards and rack or case)	
Electrical	connector resistance
Magnetic	board cross-coupling noise
Mechanical	rigidity of guide slides
Thermal	heat transfer from board to back-plane
Pathway (through the rack or case)	
Electrical	back plane wiring resistance
Magnetic	EMI radiation and shielding
Mechanical	rigid frame to avoid twisting of boards
Thermal	obstructions and rack aerodynamics

Developing the Technology Roadways

The final step in utilizing the framework is to identify the action to be taken by relating the issues to a prioritized list of future *User Requirements*. For example, old technology is to strategically position fans in a rack housing (Level-4) with properly adjusted air flow to not exceed certain *maximum temperature*. However, this may not meet future thermal density [*user*] *requirements* in the housing.

Technology questions for a road map arise when *User Requirements* cannot be met with present technology. Do the fans become the focus for technological innovation for greater air flow? Are the boards the focus for innovation in materials spread heat more efficiently, or focus on the 'first-level' components for greater heat transfer? The framework allows an "all of the above" answer and provides a systematic approach. Also, innovation can be sought for the highest leveraging solution.

The above is one obvious roadway to solving the *thermal* problem. Another roadway would look at solving the thermal problem through changes in different energy forms. A *chemical* other than air could fill the housing. Advanced magnetic shielding with high voltage withstand [*electrostatic*] coatings may allow the boards to be moved closer. Development of new electrical circuits that have less energy loss would allow higher thermal density. The change in electrical circuits to solve thermal problems is now typically done.

A final roadway would use advanced technology to combine levels. This is the continual move toward integration and mono-material systems. Chip on board is common today, combining Levels 1 and 2. A glob-topped silicon wafer with patterned edge connectors set into a special zero-force connector, may be the next 5V:1.3V dc-dc regulator. This combines Levels 1 and 3.

As a roadmap develops, hopefully, many roadways will become event. Once the roadways are identified and given a timeline and cost, it will be the industry's

responsibility to determine the direction of the journey to evolve the *power electronics packaging technology*.

Summary

A *packaging technology framework* is described that offers a systematic method to link technical packaging issues to *User requirements*. The framework has a number of uses. First, it provides a comprehensive list of technical issues that can be prioritized for technology development. Secondly, it can be used to predict packaging trends. Thirdly, it systematically establishes present design, technology and user profiles.

Beyond a technology framework, it is a tool to allow designers insight into the interrelationships of packaging, thus, allowing designers to produce an optimized systems-level packaging design. The framework facilitates the development of a common knowledge base.

The framework is divided into a four-dimensional coordinate of User Requirements, Levels of Packaging, and Technical Issues, cross-cut by Energy Forms. The *User Requirements* are derived from user clusters which are classified by the impact they have on technology drivers. The *Levels of Packaging* follow established divisions in telecom and computer electronic packaging, but are extended to five levels which traverse chip-in-package to multiple cabinets in a room.

The last axis in the framework offers a systematic method to identify the *Technical Issues* related to the energy flows along the interfaces and pathways. The *Technical Issues* are the core of the framework and allow the identification of technology development needs.

Examples assist the reader to apply the framework in the development of a *power electronics packaging roadmap*. Once roadways are identified, industry can, then, determine the direction of the journey to evolve the *power electronics packaging technology*.

References

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