Optimally Selecting Packaging Technologies and Circuit Partitions Based on Cost and Performance

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Abstract

Most power electronics circuits are packaged using two or more power electronics packaging technologies. To optimally select and use several technologies that meet performance requirements at minimum cost requires a strategic partitioning of the circuit. Presented is a structured technique for optimally selecting technologies based on a relative cost diagram. Other factors, such as performance, product volume and modularity are included.

I. Introduction

Most circuits are designed using only one or two packaging technologies that designers have intimate familiarity with. The technologies are characterized and reduced into pseudo-design guides to expedite design speed. Two commonly used technologies are plated-through-hole (PTH), glass-epoxy laminate (FR-4) and surface mount (SMT) FR-4 which allow fairly straight forward circuit partitioning. Provided the technologies meet or exceed the design needs, other technologies are not fully considered. However, when requirements are no longer met or an organization is considering future expansion, other technologies need evaluation, looking at both technical attributes and cost with cost being the dominate criterion.

Assessment of a technology is relatively easy based on technical performance. Considerable literature exists characterizing packaging materials and processes, and the recent study on the Status on Power Electronics Packaging (STATPEP)[1] identifies metrics to further evaluate the relative technical merits. Given the criterion that 'merits must meet or exceeded the requirements', partitioning of the circuit is straight forward.

There is significantly increased difficulty in evaluating more than two technologies, for the same product design, since higher performing technologies offer technical duplication over the others. The duplication geometrically increases the parameter trade-offs and appears as wasted packaging cost. To optimize the use of multiple technologies, the circuit must be optimally *partitioned* based on cost and performance.

This paper presents a structured method to circuit partitioning by combining various packaging technologies to minimize cost. A full-cost model for various technologies is developed and a comparative cost diagram produced. The diagram allows intermixing of high and low performance technologies based on surface density, which is interpreted as circuit area and, hence a partition. The method is applied to a 2.2 kW motor drive module product.

The method is also applied to product modularization, i.e., system partitioning where a specific electrophysical function is used across several products. A module can represent functional integration within a packaging technology or use multiple packaging technologies to create integrated power modules (IPMs) or power electronic building blocks (PEBBs). The importance of modularization is to increase product volume to lower cost. The cost model includes variations based on volume.

This approach to partitioning provides the criteria for matching "User Requirements" to "Levels of Packaging" as defined in the "Framework for Power Electronics Packaging"[2] proposed in earlier works. This method allows the optimum combination or integration of packaging levels for a product. The Framework, then, points to the critical technical issues that need to be considered in the technical performance. As with the Framework, this partitioning approach looks at electrical, thermal and mechanical issues (multiple energy forms).

II. The Packaging Tasks

Figure 1 shows the electrical partitions for a 2.2 kW ac motor drive and the distributed power losses. The packaging task involves different components with different functions ranging from fine-line control to high-current, high-loss power processing.

Several packaging approaches can be pursued. The Line -communications and Motor-control Blocks can use a signal-level packaging approach, such as epoxy-glass (FR-4) or insulated-metal substrates (IMS). If the Power Supply and control blocks are to be combined, an SMT approach cannot accommodate bulky storage components in the power supply.

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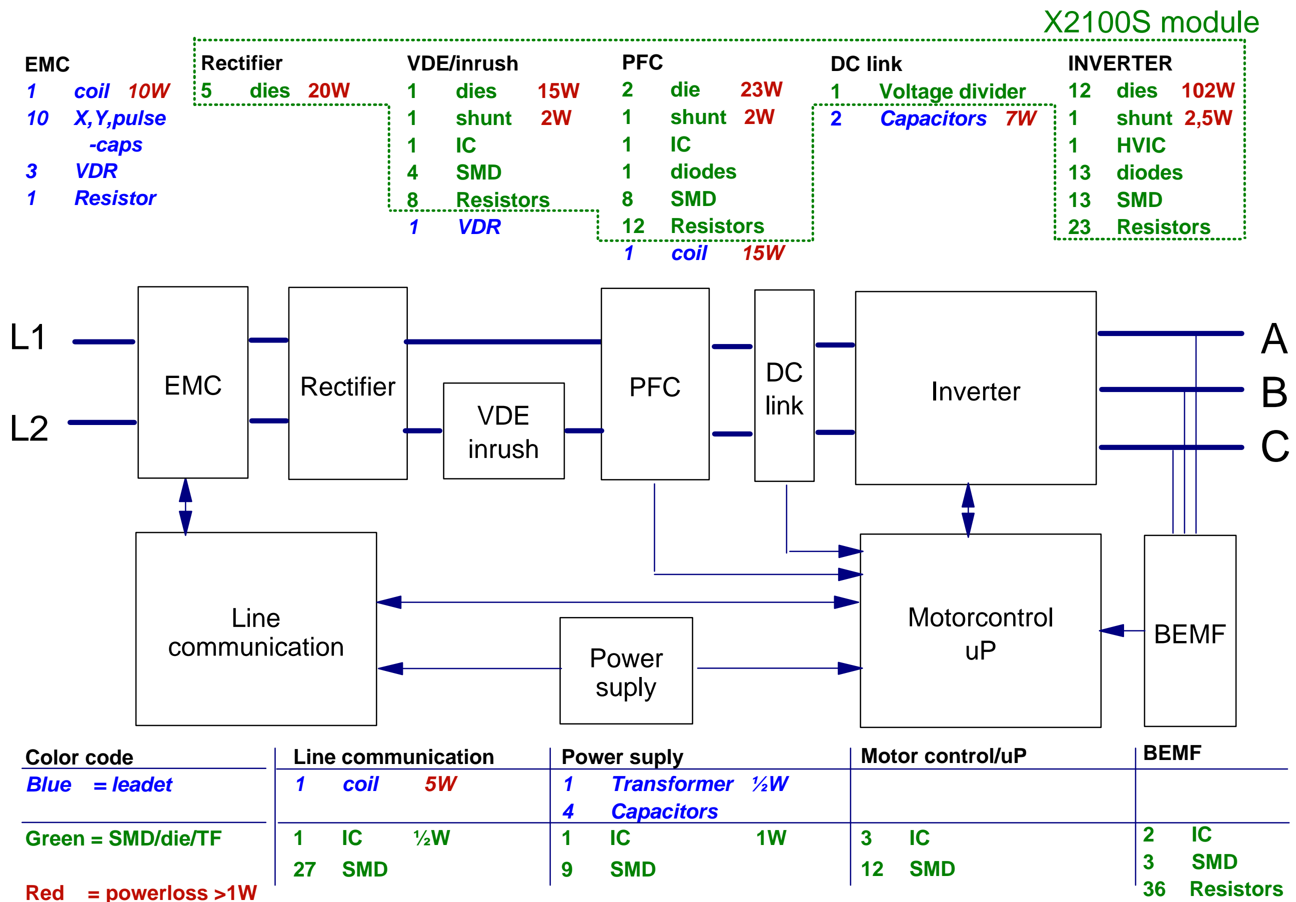

Figure 1. Electronic system with X2100S module outlined.

Hence, a through-hole approach is considered for part or all of the two blocks.

A molded interconnect (MID) approach can be considered as a less expensive approach provided the frequency response of the circuits are low and volumes high. The gate drive circuits in the power inverter stage can be accommodated by the through-hole approaches above, but may require thermal management beyond that required for control. The power components could use an IMS or copper-on-ceramic approach and also accommodate the gate drivers if SMT and/or chip-and-wire is used. An FR-4 approach can be used if a higher level of packaged components are considered and thermal components, such as heat sinks or power SMT are included as components on single-sided substrates.

A. Setting User Requirements

Such tradeoffs can be nearly endless. A structured method needs to be used to establish essential requirements and guide circuit and system partitioning. The method described here is based on characterizing and grouping the components, evaluating the cost and technical constraints, and then, matching packaging technologies to the groupings. All this is set against a set of comprehensive user requirements.

Effective systems design, including packaging, relies on accurate and comprehensive User Requirements that are established through a formal structure. A brief review is presented here. The requirements are divided into five business taxonomies that can be considered comprehensive. These are: Financial, Environmental, Legal, Social and Technical. The taxonomies are matrixed with three characteristics of requirements: Assumed, Articulated and Unexpected. Assumed Requirements are basic requirements for a product, process or service to be acceptable to all end users. Articulated Requirements discern one user from another. The Unexpected Requirements are exciters that make the product, process or service unique and competitive. Of the above, only Technical, Articulated, User Requirements are used in this paper.

The Technical requirements are further categorized to reflect the electro-physical nature of packaging. The categories are: chemical, electrical, magnetic, mechanical and thermal. Relating the requirements to all relevant energy forms provides a comprehensive listing. The energy forms are limited to electrical, mechanical and thermal in this paper.

The readers is invited to expand the comprehensiveness of the requirements by considering the other forms.

B. Steps to Partitioning

A first step to partitioning is creation of a comprehensive categorized list of electrical, mechanical and thermal, technical User Requirements. This is performed as mentioned above and as shown in Table 1 (at the end of this paper).

The second step is creation of a simple Component Characterization Map that identifies dominate attributes of the components. The block diagram of a 2.2 kW submersible pump motor drive is shown in Fig. 1 and part of the characterization map is give in Table 1. The map is divided into metrics by energy form to categorize and record extreme operating values for each component. Not all blocks need to be completed or components included, only those that most impact the technology selection. For example, any 5V, <0.1W resistor in the control circuit need not be listed since it is accommodated by nearly all technologies (e.g. as 0806, SMT, PTH, thick film, etc.). For each of the remaining components, all the mechanical package formats should be listed under the *Carrier Form*.

The third step is to strategically group components by *Carrier Form* taking into consideration limits on electrical and thermal operating points. This first-cut grouping brings a high level of packaging integration to the system and is a critical step. Similar components from all parts of the circuit become associated.

The fourth step uses the User Requirements as constraints along with engineering experience to re-associate components into different groupings. Not all components are easily regrouped. The un-associated components become dominate factors during technology selection. As an example, the high-voltage components of a bootstrap gate-drive supply can be associated with the gate drive circuit board or the high-voltage power inverter components. Interestingly, most un-associated components reside at the interfaces between functional blocks (as shown in Figure 1).

The fifth step is to map the groupings of components to the packaging technologies. This was partially performed in the previous step as engineering judgment guided the regrouping. Refinement of the selection comes when the un-associated components are incorporated. Steps four and five become iterative to provide optimum partition(s).

III. Characteristics of Packaging Technologies

There are many technologies applicable to packaging of medium to high volume power electronics systems with application areas ranging from appliances and transportation to computer and telecom. Each technology is briefly described and the main attributes noted. High-cost, high-performance technologies typically used in military and space applications are not considered.

The technologies are divided by the delivery form, i.e. mechanical support structure which exists in the electrical interconnect layer (e.g. bus bars), electrical isolation layer (e.g. ceramics) or a separately added thermal conduction layer (e.g. AlSiC baseplates). The delivery form is an important aspect since the size of mounted components greatly limits the choices in technologies. The more mechanically robust the technology greater the mass of the components that are accommodated. The technologies reviewed below sequentially range from robust to allow for clamped, screwed and axially leaded components to modestly robust for surface mounted components. The transition from plated through holes (PTH) to surface mount technology (SMT) occurs within FR-4 and partly explains the greater acceptance of this versatile technology.

Laminated Bus-Bar - A polymer, such as epoxy, glues together thick conductor bars while providing electrical isolation. The bars can be free-floating laminated interconnects or, if sufficiently thick, be the metal carrier. Vias between layers are metal posts or fasteners placed through drilled or stamped holes. These are used in high current systems and can accommodate very large components. These were not considered in this development.

Molded Interconnect Device (MID) - A high temperature plastic or polymer structure hosting electrical interconnects is fabricated by 1-shot, 2-shot or insert molding. The interconnections are formed by hot-stamping copper foil, imaging and metal plating the polymer, or insert-molding of structured metal. MID lends itself to high volume, 3-D, net shape packaging and is extensively overlooked in the power electronics area (excluding automotive). Components can be surface mounted or through hole with moderate to course line resolution. Only the hot embossing is considered here.

Glass-Epoxy with plated through holes (FR-4, PTH) - A fiberglass mesh is impregnated with epoxy and metalized with copper. Interconnect patterns are etched into the foil. The patterned copper clad mesh can be laminated and vias formed by drilled and plated holes. Leaded components are attached by soldering leads that have been placed through holes.

Glass-Epoxy with surface mount pads (FR-4, SMT) - Same as above except chip components are solder attached.

Insulated Metal Substrate - polymer on metal (IMS-PM) - A polymer is used to isolate and attach a conductive interconnect to a metal plate which provides mechanical support. Vias can be placed between the interconnect and plate and a layer of polymer and interconnect can be attached to the interconnect layer.

Insulated Metal Substrate - steel corded (IMS-PS) - A high temperature glass (~900°C) coats a steel plate and a thick-film conductive cermet interconnect is applied upon the glass. The structure is similar to traditional thick-film. Vias are processed as in multilayer thick-film.

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Thick-Film on Ceramic - Glass based pastes or inks are loaded with electrically conductive materials, such as copped, gold or silver, to form interconnects; with resistive materials to form components; or used unloaded as dielectrics. The pastes are screen printed on ceramic and fired at ~900°C. Vias are formed as holes in dielectric layers and discrete components are surface mounted with solder or adhesives. Only two types of air fired thick film are considered here: Multilayer Thick Film (TF-multilayer) for control circuity and Thick Thick Film(TTF) where silver is printed to form up to 160 µm conductors for power.

Plated Cu on Ceramic (Z-Strate) - patterns are imaged or transferred to the surface of ceramic. Copper is then plated to a thickness <125 µm (5 mils). Discrete components are attached or full thick-film processing is placed on the plated copper with screen-printed components imbedded or discrete components attached.

Direct Bonded Copper (DBC) - Copper foil is applied to ceramic, bonded at ~1063°C, and a pattern is etched. Discrete components are surface mounted with solder or adhesive. There are no vias.

IV. Full-Cost Model

When discussing cost it is necessary to define centers of cost and business. The following terms will be used:

1. Materials cost
2. Production cost
3. Partitioning cost
4. Full cost
5. Product business cost (return on investment for development of one product)
6. Company business cost (return on investment for cross products)

1. *Materials cost* represent direct costs of packaging materials. The variation in cost by volume must also be included. Volume dependency is biggest for custom products at low volume and lowest for standard high volume products. A typical volume cost factor is 20% decrease in cost per 10 fold increase in volume.
2. *Production cost* includes factors for wages and product volume, but are independent of material costs (which is not often assumed when assessing overhead). Production cost can be characterized as a function of technology and quantity. To reflect this into a design tool, it is necessary to describe production cost as a function of simple information, such as the number of SMD components and leaded components and square inches of substrate board. Assessment is as follows for a captive production:
   1. Determine the total wages, equipment and facility depreciation, and other facility overhead.
   2. Determine the number of production technologies in the facility, both in place and available with minimal extension.
   3. Determine technology costs by a ratio of the above two parameters.
   4. Add scaling factors for volume dependency

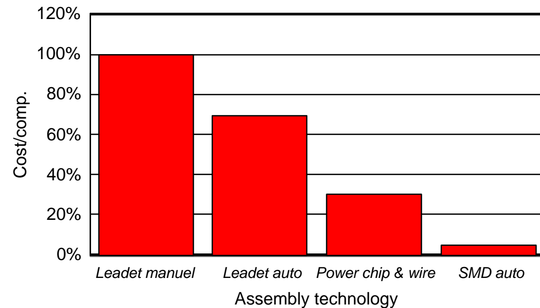

Figure 2. Relative production cost for assembly technologies

In Fig. 2 relative production costs for various technologies is shown for fixed volume. Note that chip & wire is less expensive than handling a leaded component which is typical for captive facilities. Including scaling factors in your calculations may give volume dependency as shown in Fig. 3 for a highly automated production technology. Depreciation is for production equipment and buildings, whereas other overhead covers the significant cost involved in purchasing, management, production technology etc.

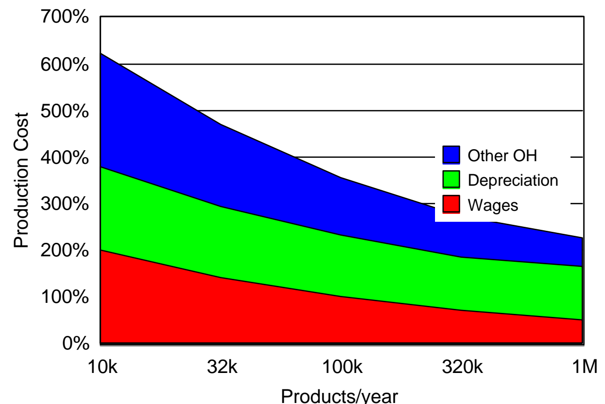

Figure 3. Production cost dependency on volume

3. *Partitioning cost* is incurred for each technology used. From the previous technology descriptions it appears straight forward to chose “this technology for these components and those technologies for those components” based on *technical* performance attributes. However, there is a drawback to this partitioning. Each partition adds one circuit to be handled through production with an additional interconnect and assembly process. This means additional incremental costs. Assembling subcircuits into a product is similar to assembling components on boards and is modeled as cost

in wages modified by a different overhead factor. For chip & wire, costs for protecting (encapsulating) chips, are included if necessary.

4 *Fullcost* combines material costs and production costs as shown in Fig. 4. A minimum-packaged-component system is chosen to highlight the possibility of buying non-packaged components, but the model is valid for any level of packaging. If there is not a captive circuit fabricator, then, the cost is obtained through competitive quotes or experience with the manufacturer. A mixture of in-house and out-sourced costs can be included in themodel.

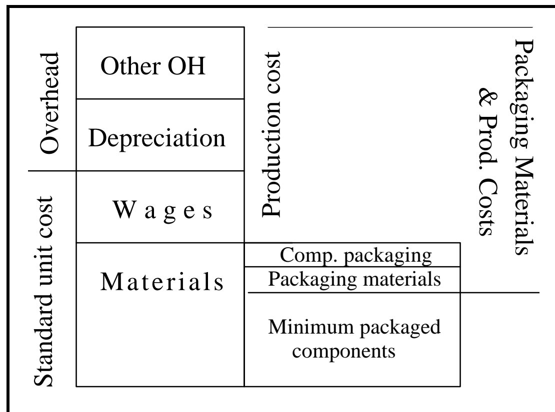

Figure 4. Full Cost Model for production

5 *Product business cost*, i.e. return on investment for development of one product, is an investment in future payback. The total cash flow from development until end of production determines the business costs for a product as illustrated in Fig. 5.

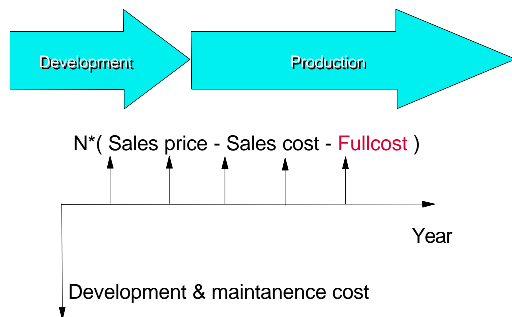

Figure 5. Product business cost for product

6 *Company business cost*, i.e. return on investment for cross products, reflects the cost of optimization across products. The value of reusing the same packaging technologies, designs (diagrams) and even physical circuits (building blocks) across different products should be measured at the company level. The value of building blocks becomes obvious through savings in repetitive development costs and maintenance of function. Development and maintenance costs are saved since the function is only developed once, and unilaterally maintained across all products.

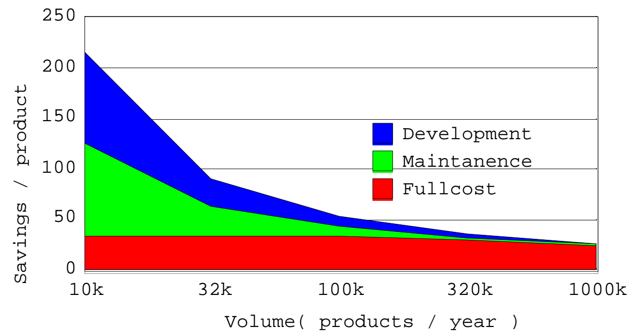

Figure 6. Value of building block

The impact of volume on building block cost applied to three motor drive products is shown in Fig. 6. At low volumes the main savings are in development and maintenance costs, while at high volumes only savings in fullcost matters. The overall conclusion is that if a partition is necessary to meet requirements, then, the partition must be guided by strategic choices in order to optimize cost on a company business level and relative cost diagrams should be used only for optimizing within partitions.

V. Partitioning Approach

There are several interrelationships that have evolved which naturally aid partitioning. Rank ordering common packaging technologies by technical performance, also orders most other attributes. As one moves down the list of technologies described in the above section, one finds that, in general, there is greater electrical performance (higher current carrying capacity, higher voltage isolation and higher operating frequency), greater thermal performance (thermal conduction and transient heat management), higher density (finer lines, except DBC), more sophisticated processing, and higher cost.

These monotonic trends have provided a natural taxonomy for development of rich engineering judgment which can be used to effectively group components (step four in Section II above) for optimized partitioning.

Iterations of the last two steps, in Section II, can be minimized by following a sequence of first matching the most challenging component grouping with the higher performance technology. The next challenging grouping is matched with the next technology of lower, but suitable, performance and lowest cost. Starting with the highest performance technology also allows much lower component groupings to be considered for inclusion at possibly no increased cost. For example, if Ceramic Thick Film is used for chip and wire power die and current sense resistors, the inclusion of thick film control circuits comes with little added real estate (cost).

A graphical perspective on this is provided in Fig. 7 and is only briefly discussed here. The falling curves represent relative cost of each technology as area changes. The starting and ending points are the practical limits in the use of the technology at certain densities.

It is recommended the curves be viewed right to left (as density decreases). As an example, assume a given circuit is designed with only one technology, such as thick film (TF), and as dense as possible. As board area increases (becoming less dense), components can grow in size (0603 to 0805) with larger interconnect traces. The cost increases, following the curves up and to the left. With increased area and cost, cheaper technology may be suitable, such as SMT FR-4. This other technology would decrease cost for the same area. Hence, cost, density and performance decrease. However, within a range near maximum density, the higher performance TF technology with added area is still *less costly*. This is due to *packaging and production costs*, and is often overlooked by designers who look at cost per square area of boards without looking at the full cost model. A more generalized set of curves is shown in Fig. 7 which can be quantified for specific production and to guide partioning.

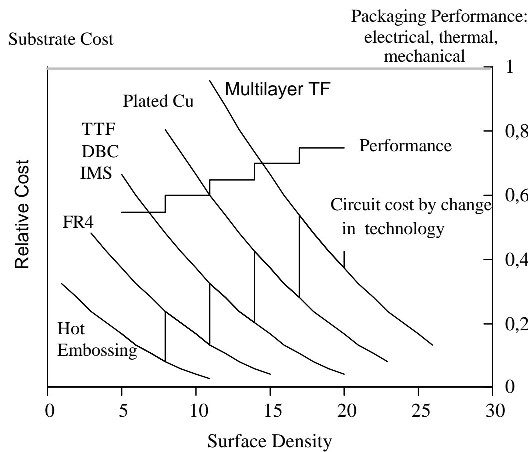

Figure 7. Relative cost relationships of technologies

VI. A 2.2 kW Motor Drive Design

A 2.2 kW submersible pump system, consisting of electronics, motor and pump encased in one housing, is used as an example product. The block diagram of the electronics is shown in Figure 1. For a planar electronic circuit assembly, the physical assembly pattern would closely follow the electrical schematic layout and one packaging technology cold be used, though not efficiently. However, in multiple assembly planes, as provided with mixed packaging technologies, the assembly pattern more closely follows groupings of the physical carrier forms of the components. The steps outlined in Section II - The Packaging Tasks, given earlier, are followed to determine the proper partitioning of the system to meet performance requirements and provide maximum business profit. The steps are summarized as:

1. User Requirements
2. Component Characterization
3. Component Grouping
4. Strategic Partitioning with constraints
5. Optimizing within partitions

A. *User Requirements (constraints)*

There are many user requirements that direct the system design as outlined in Section I. However, several requirements place specific constraints on the packaging of the 2.2 kW drive as noted below.

1. Mechanical: To be built into stainless steel tube with a diameter of 65mm, as short as possible.
2. Thermal: Cooling through tube with non-flow of water at 30°C.
3. Environment: Potting complete electronics inside tube not allowed
4. Regulatory: UL, CE
5. Reliability: 1.000.000 quick start/stop
30.000 max gradient start/stop
40.000 h lifetime @ 10°C water

B. *Component Characterization Map*

A Component Characterization Map is performed on all the components which identifies dominate technical and physical attributes, and are recorded as in Table 1. In this Component Characterization Map components are listed for each electrical functional block

C. *Component grouping*

An overview of possible groupings into packaging partitions is obtained by attaching main components and key attributes to the functional block diagram of Figure 1.

D. *Strategic Partitioning with Constraints*

A major constraint is the limited space available (65 mm diameter). This makes it obvious that some miniaturization is very valuable, but what should be miniaturized? Leaded components cannot be miniaturized by packaging. These components require either PCB (for soldering) or some form of lead frame (MID for welding). Power die are top candidates for miniaturization because the die can be grouped into a power module that is much smaller than discrete power components. Also, high power losses do not allow the same packaging technologies to be used as for leaded components.

The remaining non-power die and associated components are prime candidates for modularization. Highest value is reached if a building block can be reused across different products. Therefore, as much control circuitry as possible should be integrated without violating the possibility for reuse in other products. For this product, the line communications bus and motor control circuitry would be excluded, but the control for VDE/inrush and PFC would be integrated together

with the driver and all sense resistors. This integrates 82% of all power losses for easier cooling, integrates all power-component-dependent control circuity, and enables product-independent maintenance and power die optimization.

At this stage there are usually new requirements added for cross product reuse. In this case another application requires 125°C baseplate temperature.

E. Optimization within Partitions

Optimization requires choosing optimum technologies to meet cost and performance requirements. Figure 8 shows relative cost of various substrates together with the cost of suitable production technologies. Note that the substrate cost is for equal substrate area but different performance, e.g. IMS requires more space for control circuity than TF multilayer because IMS has only one conductor layer at a cost indicated in Fig. 8.

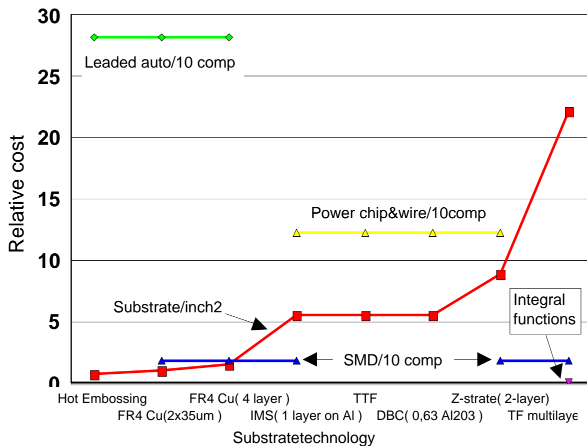

Figure 8. Technology costs

Figure 8 should be used together with Fig 1 which shows that the module includes both Power Chip & Wire (PC&W) and low power control circuity (SMT). The PC&W can be accommodated by DBC, IMS, TTF and Z-Strate. Fine line SMT can be accommodate by FR4, IMS, TF multilayer and Z-Strate. This should initially lead to the conclusion that DBC, IMS or TTF should be used for power, excluding Z-Strate due to cost; and FR4 for control, excluding the others due to cost.

Are all cost issues taken into account and all requirements meet? Not necessarily. Component cost is influenced by packaging approaches. Power sense resistors, which are typically in SMT form, can be integrated in TF multilayer at near zero incremental cost. Also, less expensive integrated circuits can be chosen when the packaging approach allows active trimming of associated components. Besides cost, technical issues limit packaging choices for certain circuit partitions. Reliability and temperature requirements (125°C) rule out FR4.

There are fewer and fewer choices. If power die were available as known good die, then power and control could be combined on one substrate with IMS or Z-Strate. The IMS has drawbacks, such as lower power cycling capability due to a high TCE and is only a one-layer technology which means more area and less noise immunity. Z-Strate has neither of these problems, but due to lack of known good power die was not chosen. Also, Z-strate does not allow component integration at the cost indicated in Fig. 8. A two substrate solution was needed.

Power DBC was chosen as the obvious highest performing technology among comparable low cost power substrates. The DBC is soldered onto a low cost copper base that extends to form a mounting base for the control substrate.

Multilayer thick film was chosen for control circuity despite the apparently high *substrate cost*. In the X2100S module, this substrate is the optimum cost choice because of high component integration, such as the three buried power current-sense resistors and many printed resistors for accurate active trimming of functions associated with the integrated circuits. Partitioning cost is minimized by combining interconnections of substrates with interconnection to I/O terminals in one technology -- heavy wire bonding. This has been possible by designing an MID interconnection component with terminals that are wire bondable on one end and solderable on the other. The resulting module is shown in Fig. 9.

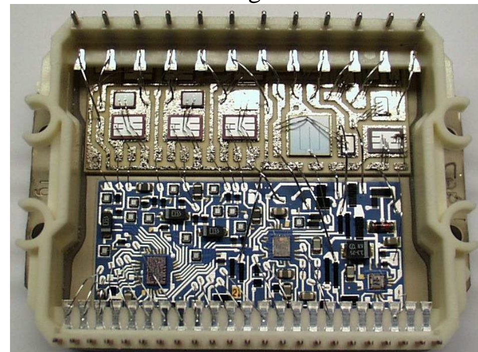

Figure 9. X2100S Module with MID housing

There are other components not best accommodated in the module and are both SMT and leaded. Therefore, a 2 layer FR4 is chosen as the lowest cost technology that is suitable for both carrier forms. Mechanical stability and cooling is achieved by using a patented structure of extruded aluminum profiles. In Fig. 10 the disassembled motor with integrated frequency converter are shown, and in Fig. 11 the resulting product for the end customer is shown. The Fig. 10 construction is very compact and the miniaturized X2100S building block allowed remaining circuity to be on one PCB.

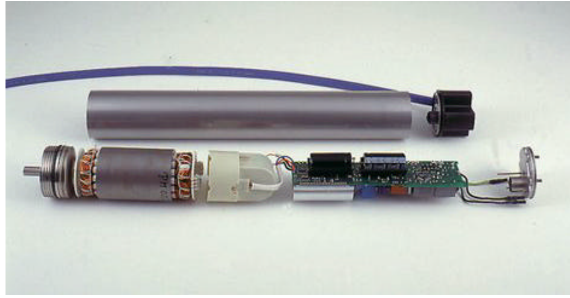

Figure 10. Motor with integrated frequency converter

Using bare die, higher cost substrates and partitioning with different technologies allowed the value of the product to surpass cost targets**.** The value of choices for packaging levels 1 and 2 address optimization of *product business cost* as defined in Section IV. Designing the building block as a component for reuse across other products increases volume and reduces cost. More importantly, relative low volume products can benefit from the building block by faster development cycles, lower development cost, lower level-3 packaging cost and lower maintenance cost. The building block value addresses optimization of *company business cost*.

This is an example of how miniaturization at very low cost has contributed to a unique product. This 3 inch diameter pump replaces the much longer 4 inch pump by running at higher speeds enabled through the built-in frequency converter. Figure 11 shows the finished product, which in the field is known as the SQ pump.

Figure 11. The SQ pump under installation

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[1] M. Meinhardt, et. al., “STATPEP-Current Status of Power Electronics Packaging for Power Supplies - Methodology,” Proc. of the 14th Annual Applied Power Electronics Conference and Exposition, pp 16-22, March 14-18, 1999.

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Table 1. Component Characterization Map

Funct block	Function	Comp	Qty	Mechanical		Electrical			Thermal		
				Delivery-form	Size	Voltage	Current	Constraint	Powerloss	Max temp	Rth
						V	A/comp		W/comp	degC	K/W
EMC	Filter	Y-cap	2	leaded	13x5x10	300 ac		low L to earth			
	Filter	X-cap	2	leaded	26x10x18	300 ac		low L to L1-L2			
	Choke	inductor	1	leaded	ø37x20	300 ac	11 rms		6	105	
	Filter	X-cap	1	leaded	17x6x12	300 ac		low L to earth			
	Transient clamp	VDR	3	leaded	ø21x5	300 ac		1 low L to L1-L2 2 low L to L-Earth			
	Filter	Y-cap	2	leaded	18x9x15	300 ac		low L to earth			
	Filter	Y-cap Resistor	2 1	leaded leaded	12x8x10 ø4x10	300 ac		low L to earth			
	Puls	MKT	1	leade	31x18x28	300 ac		Close to DCP-DCN			
Rectifier	Bridge	Diode	4	die	3,5x2,5	600	11 rms		5	125	